

# Compal Confidential

## KALH0 /KAL90+ /KALG0 M/B Schematics Document

### Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2009-3-4

REV:1.0

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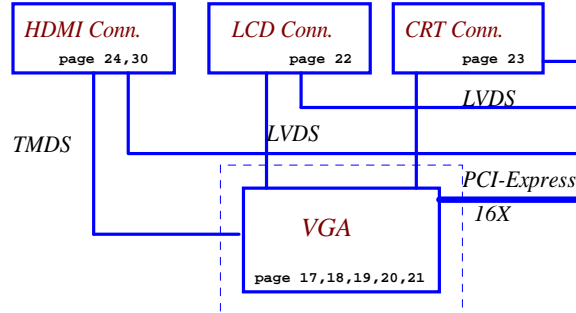
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EMC 1402  
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Clock Generator  
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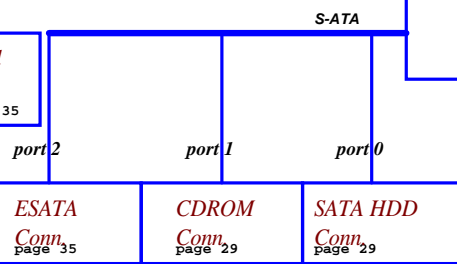
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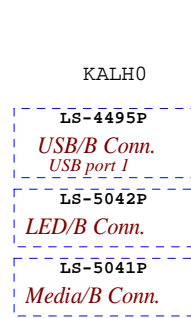
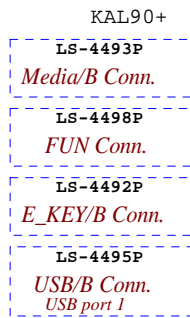
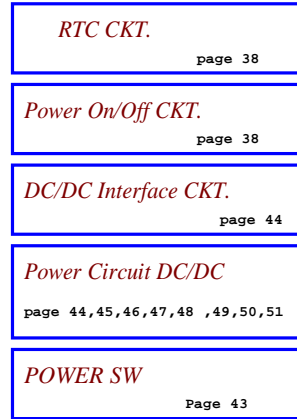
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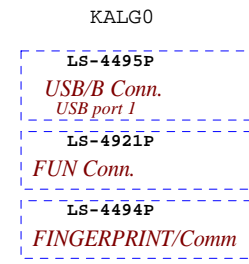
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for HDA/DDR3	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V GM LVDS MODULE	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+1.1VS	1.1V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADT7421	1001 100X b
MEDIA CONSOLE	1010 000X b	NB9M THERMAL SENSOR	

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LPRS387, SLG6SP556V)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Configuration Table

Project	BOM Configuration
KAL90-UMA	XXXXXXXXXX:KAL90@/GM@/888VC@/8121@/GM45@
KAL90-Dis	XXXXXXXXXX:KAL90@/PM@/888VC@/8121@
KALH0-GM45	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GM45@
KALH0-GL40	XXXXXXXXXX:KALH0@/GM@/888VC@/8121@/GL40@
KALH0-PM45	XXXXXXXXXX:KALH0@/PM@/888VC@/8121@
KAL90+ -UMA	GM@/888VC@/8121@/GM45@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@
KAL90+ -Dis	PM@/888VC@/8121@/KAL90+_G0@/KAL90_90+@/KAL90_G0_90+@/KAL90_H0_90+@/KAL90+_PCB@/PM45@
KALG0 -UMA (GL40)	KALG0@/GM@/888VC@/8121@/GL40@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -Dis	KALG0@/PM@/888VC@/8121@/PM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -UMA (GM45)	KALG0@/GM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@
KALG0 -DIS (GM45)	KALG0@/PM@/888VC@/8121@/GM45@/KAL90+_G0@/KALH0_G0@/KAL90_G0_90+@/KALG0_DDR2 PCB RV0 @/KALG0+@

KALG0 LAN to AR-8131----- 8121@ Change to 8131@

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra/Rc/Re	100K +/- 5%				
Board ID	Rb / Rd / Rf	VAD_BID_min	VAD_BID_typ	VAD_BID_max	
0	0	0 V	0 V	0 V	
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	




BOARD ID Table

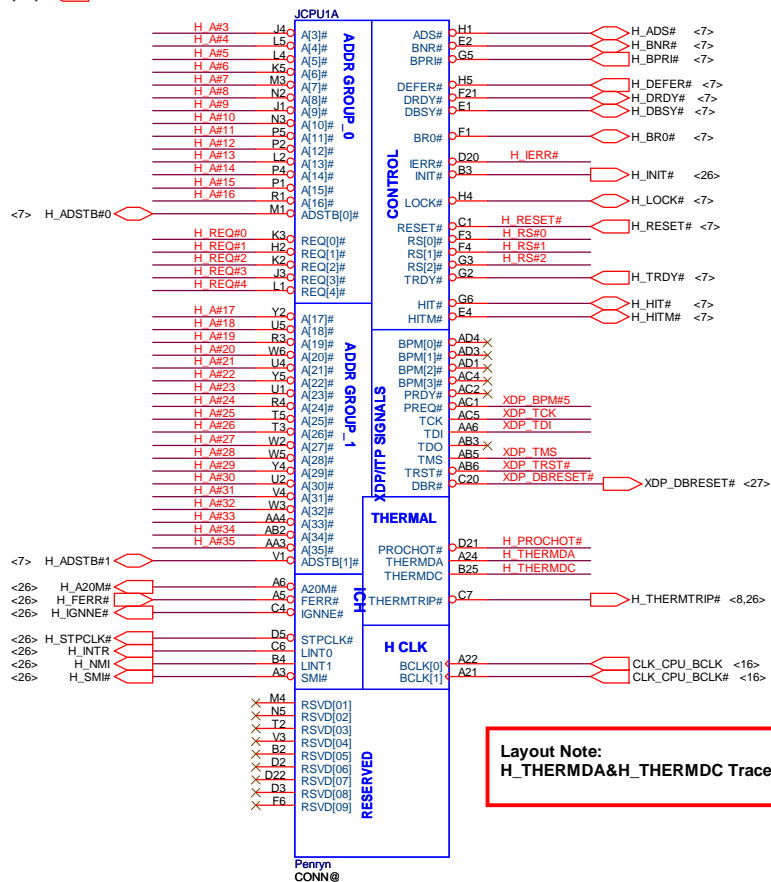
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
KAL90	KAL90@
UMA	GM@
PM@	PM@
ALC888VC	888VC@
ALC888VB	888VB@
AR8121	8121@
AR8112	8112@
ALC268	268@
GL40	GL40@
GM45	GM45@
KAL90-G0	KAL90_G0@
KAL90-H0	KAL90_H0@
KALG0	KALG0@
KALH0	KALH0@
ALC268	268@
	KAL90_90+@
	KAL90_H0_G0@
	KAL90+_G0
	KALH0_G0
	KAL90_G0_90+@
	KAL90_H0_90+@
	KAL90+_PCB@
	KALG0_PCB@

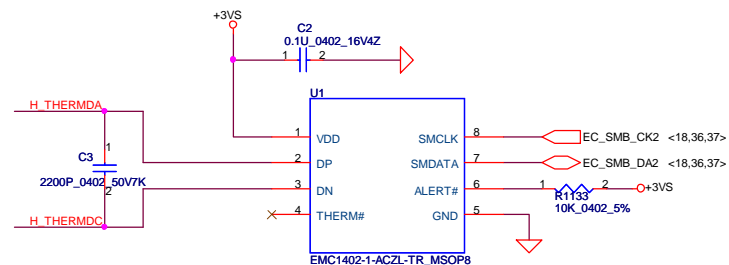
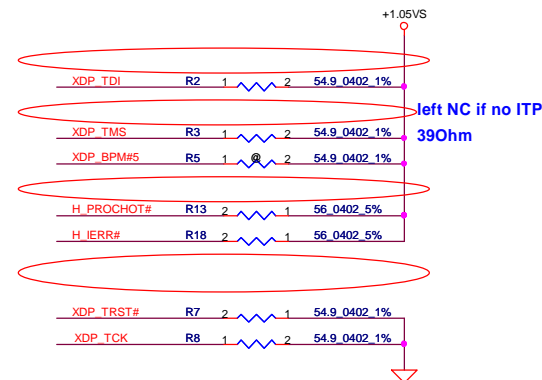
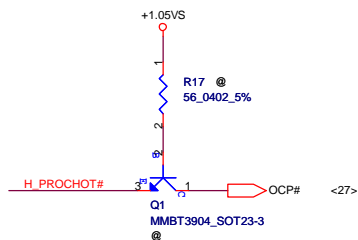
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<7> H\_A# [3..35]  H\_A# [3..35]  
 <7> H\_REQ# [0..4]  H\_REQ# [0..4]  
 <7> H\_RS# [0..2]  H\_RS# [0..2]



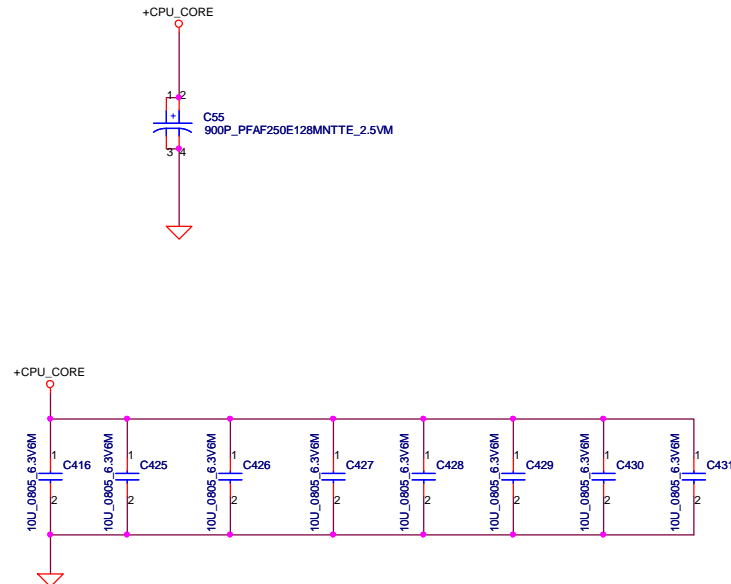
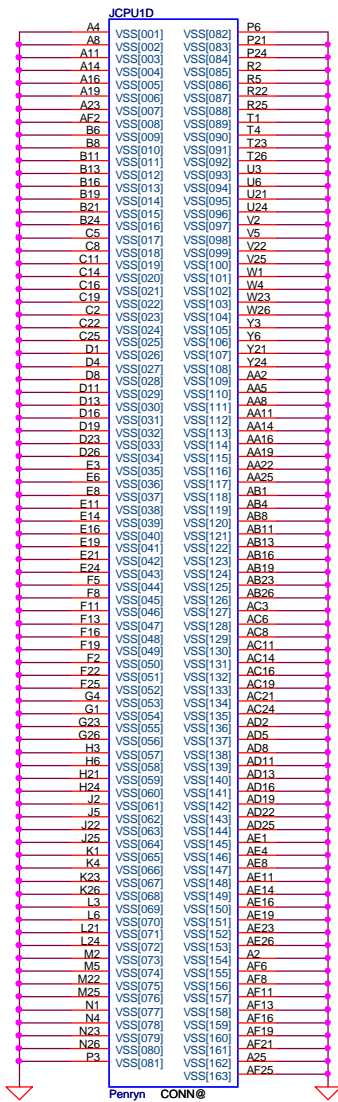
**Layout Note:**  
 H\_THERMDA & H\_THERMDC Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

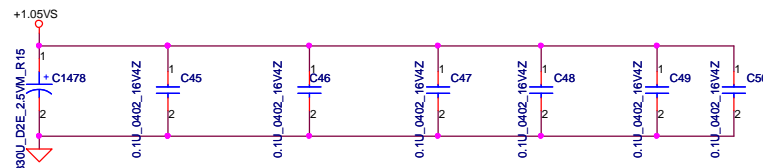


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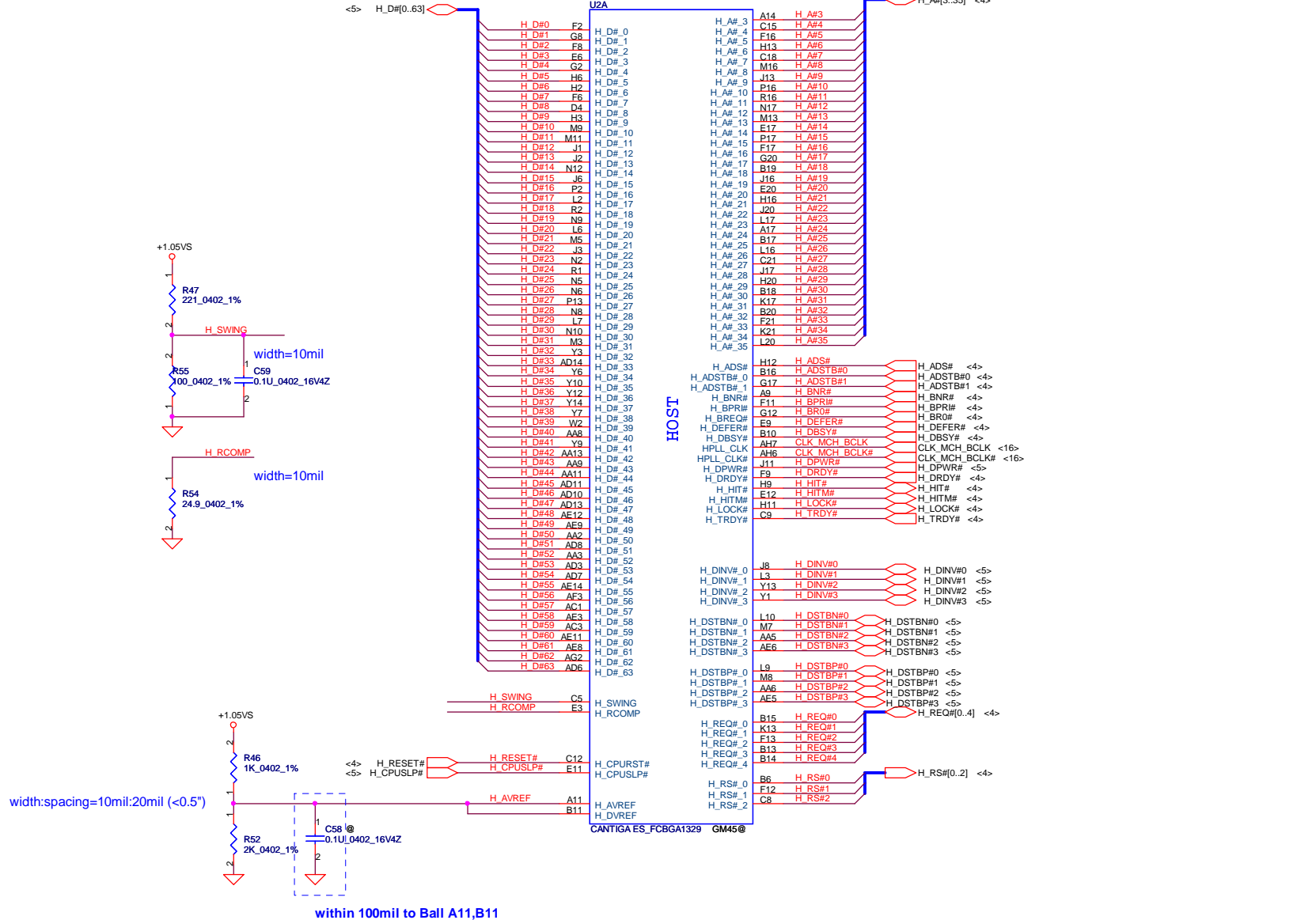




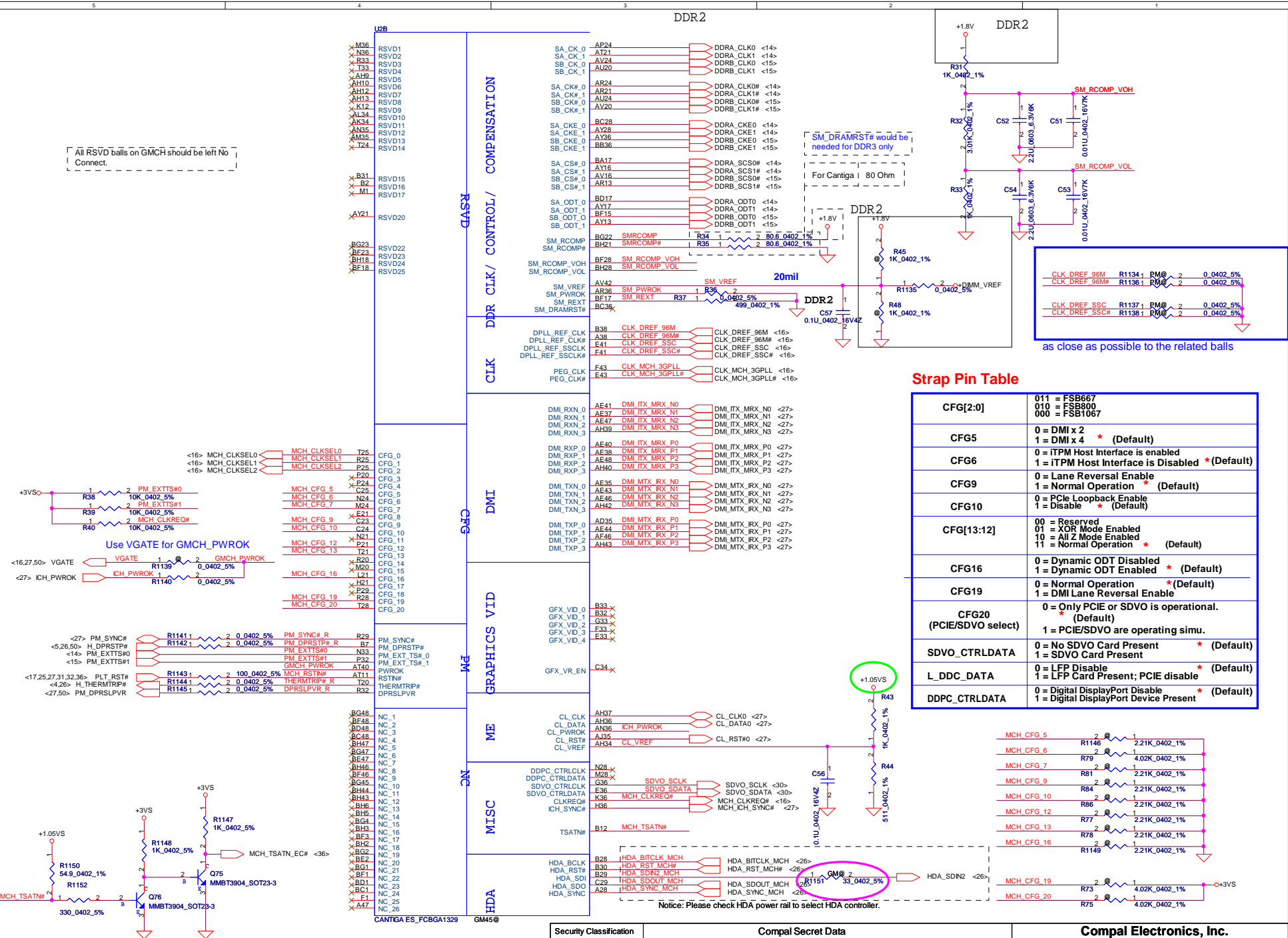
+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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<14> DDRA\_SDQ[0..63] <15> DDRA\_SDM[0..7] <14> DDRA\_SMA[0..14]

<15> DDRB\_SDQ[0..63] <15> DDRB\_SDM[0..7] <15> DDRB\_SMA[0..14]

DDRA\_SDQ0 AJ38 DDRA\_SDQ1 AJ41 DDRA\_SDQ2 AN38 DDRA\_SDQ3 AM38 DDRA\_SDQ4 AJ36 DDRA\_SDQ5 AJ40 DDRA\_SDQ6 AM44 DDRA\_SDQ7 DD4 DDRA\_SDQ8 AN43 DDRA\_SDQ9 AN44 DDRA\_SDQ10 AU40 DDRA\_SDQ11 AT38 DDRA\_SDQ12 AN41 DDRA\_SDQ13 AN39 DDRA\_SDQ14 AU44 DDRA\_SDQ15 AU42 DDRA\_SDQ16 AU39 DDRA\_SDQ17 AY44 DDRA\_SDQ18 BA40 DDRA\_SDQ19 BD43 DDRA\_SDQ20 AV41 DDRA\_SDQ21 AY43 DDRA\_SDQ22 BB41 DDRA\_SDQ23 BC40 DDRA\_SDQ24 AY37 DDRA\_SDQ25 BD38 DDRA\_SDQ26 AY37 DDRA\_SDQ27 AT36 DDRA\_SDQ28 AY38 DDRA\_SDQ29 BB38 DDRA\_SDQ30 AV36 DDRA\_SDQ31 AV36 DDRA\_SDQ32 BD13 DDRA\_SDQ33 AU11 DDRA\_SDQ34 BC11 DDRA\_SDQ35 BA12 DDRA\_SDQ36 AU13 DDRA\_SDQ37 AU13 DDRA\_SDQ38 BD12 DDRA\_SDQ39 BC12 DDRA\_SDQ40 BB9 DDRA\_SDQ41 BA9 DDRA\_SDQ42 AU10 DDRA\_SDQ43 AV9 DDRA\_SDQ44 BA11 DDRA\_SDQ45 BD9 DDRA\_SDQ46 AY8 DDRA\_SDQ47 BA6 DDRA\_SDQ48 AV5 DDRA\_SDQ49 AV7 DDRA\_SDQ50 AT9 DDRA\_SDQ51 AN8 DDRA\_SDQ52 AU5 DDRA\_SDQ53 AU5 DDRA\_SDQ54 AT5 DDRA\_SDQ55 AN10 DDRA\_SDQ56 AM11 DDRA\_SDQ57 AM5 DDRA\_SDQ58 AJ9 DDRA\_SDQ59 AJ8 DDRA\_SDQ60 AN12 DDRA\_SDQ61 AM13 DDRA\_SDQ62 AJ11 DDRA\_SDQ63 AJ12

SA\_BS\_0 SA\_BS\_1 SA\_BS\_2 SA\_RAS# SA\_CAS# SA\_WE# SA\_DM\_0 SA\_DM\_1 SA\_DM\_2 SA\_DM\_3 SA\_DM\_4 SA\_DM\_5 SA\_DM\_6 SA\_DM\_7 SA\_DQS\_0 SA\_DQS\_1 SA\_DQS\_2 SA\_DQS\_3 SA\_DQS\_4 SA\_DQS\_5 SA\_DQS\_6 SA\_DQS\_7 SA\_DQS\_0 SA\_DQS\_1 SA\_DQS\_2 SA\_DQS\_3 SA\_DQS\_4 SA\_DQS\_5 SA\_DQS\_6 SA\_DQS\_7 SA\_MA\_0 SA\_MA\_1 SA\_MA\_2 SA\_MA\_3 SA\_MA\_4 SA\_MA\_5 SA\_MA\_6 SA\_MA\_7 SA\_MA\_8 SA\_MA\_9 SA\_MA\_10 SA\_MA\_11 SA\_MA\_12 SA\_MA\_13 SA\_MA\_14

DDRB\_SDQ0 AK47 DDRB\_SDQ1 AH46 DDRB\_SDQ2 AP47 DDRB\_SDQ3 AP46 DDRB\_SDQ4 AJ46 DDRB\_SDQ5 AJ48 DDRB\_SDQ6 AM48 DDRB\_SDQ7 AP48 DDRB\_SDQ8 AU47 DDRB\_SDQ9 AU46 DDRB\_SDQ10 BA48 DDRB\_SDQ11 AY48 DDRB\_SDQ12 AT47 DDRB\_SDQ13 AR47 DDRB\_SDQ14 BA47 DDRB\_SDQ15 BC47 DDRB\_SDQ16 BC46 DDRB\_SDQ17 BC44 DDRB\_SDQ18 BG43 DDRB\_SDQ19 BF43 DDRB\_SDQ20 BE45 DDRB\_SDQ21 BC41 DDRB\_SDQ22 BF40 DDRB\_SDQ23 BF41 DDRB\_SDQ24 BG38 DDRB\_SDQ25 BF38 DDRB\_SDQ26 BH35 DDRB\_SDQ27 BG35 DDRB\_SDQ28 BH40 DDRB\_SDQ29 BG39 DDRB\_SDQ30 BG34 DDRB\_SDQ31 BH34 DDRB\_SDQ32 BH14 DDRB\_SDQ33 BG12 DDRB\_SDQ34 BH11 DDRB\_SDQ35 BG8 DDRB\_SDQ36 BH12 DDRB\_SDQ37 BF11 DDRB\_SDQ38 BF9 DDRB\_SDQ39 BG7 DDRB\_SDQ40 BC5 DDRB\_SDQ41 BC6 DDRB\_SDQ42 AY3 DDRB\_SDQ43 AV1 DDRB\_SDQ44 BF6 DDRB\_SDQ45 BF5 DDRB\_SDQ46 BA1 DDRB\_SDQ47 BD3 DDRB\_SDQ48 AV2 DDRB\_SDQ49 AJ3 DDRB\_SDQ50 AR3 DDRB\_SDQ51 AN2 DDRB\_SDQ52 AY2 DDRB\_SDQ53 AV1 DDRB\_SDQ54 AP3 DDRB\_SDQ55 AR1 DDRB\_SDQ56 AL1 DDRB\_SDQ57 AL2 DDRB\_SDQ58 AH1 DDRB\_SDQ59 AH1 DDRB\_SDQ60 AM2 DDRB\_SDQ61 AM3 DDRB\_SDQ62 AH3 DDRB\_SDQ63 AJ3

SB\_BS\_0 SB\_BS\_1 SB\_BS\_2 SB\_RAS# SB\_CAS# SB\_WE# SB\_DM\_0 SB\_DM\_1 SB\_DM\_2 SB\_DM\_3 SB\_DM\_4 SB\_DM\_5 SB\_DM\_6 SB\_DM\_7 SB\_DQS\_0 SB\_DQS\_1 SB\_DQS\_2 SB\_DQS\_3 SB\_DQS\_4 SB\_DQS\_5 SB\_DQS\_6 SB\_DQS\_7 SB\_DQS\_0 SB\_DQS\_1 SB\_DQS\_2 SB\_DQS\_3 SB\_DQS\_4 SB\_DQS\_5 SB\_DQS\_6 SB\_DQS\_7 SB\_MA\_0 SB\_MA\_1 SB\_MA\_2 SB\_MA\_3 SB\_MA\_4 SB\_MA\_5 SB\_MA\_6 SB\_MA\_7 SB\_MA\_8 SB\_MA\_9 SB\_MA\_10 SB\_MA\_11 SB\_MA\_12 SB\_MA\_13 SB\_MA\_14

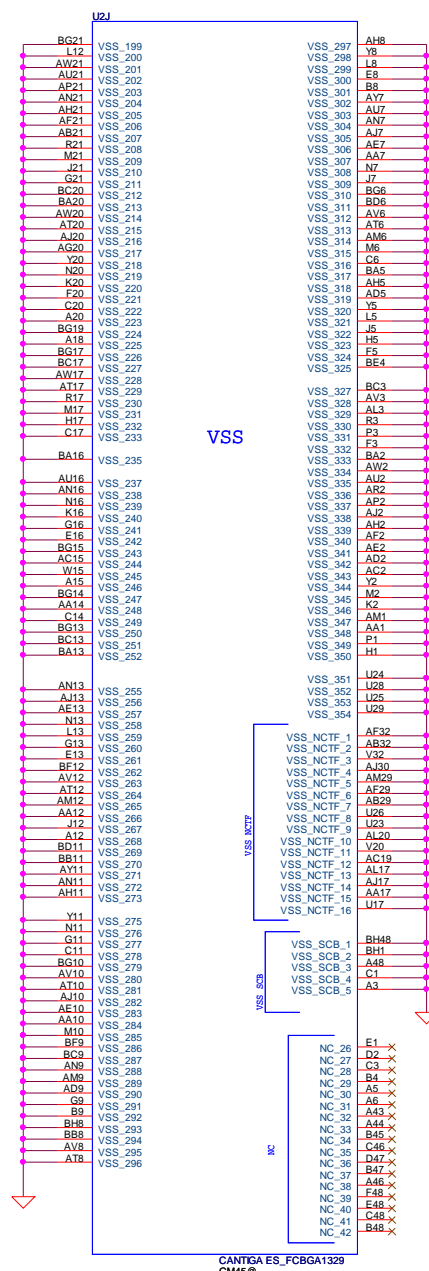
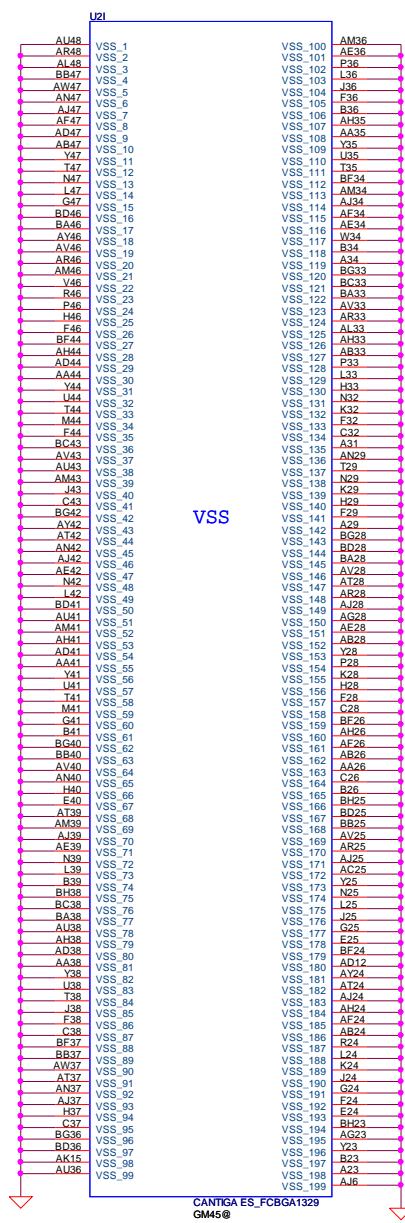
CANTIGA ES\_FCBGA1329 GM45@

CANTIGA ES\_FCBGA1329 GM45@



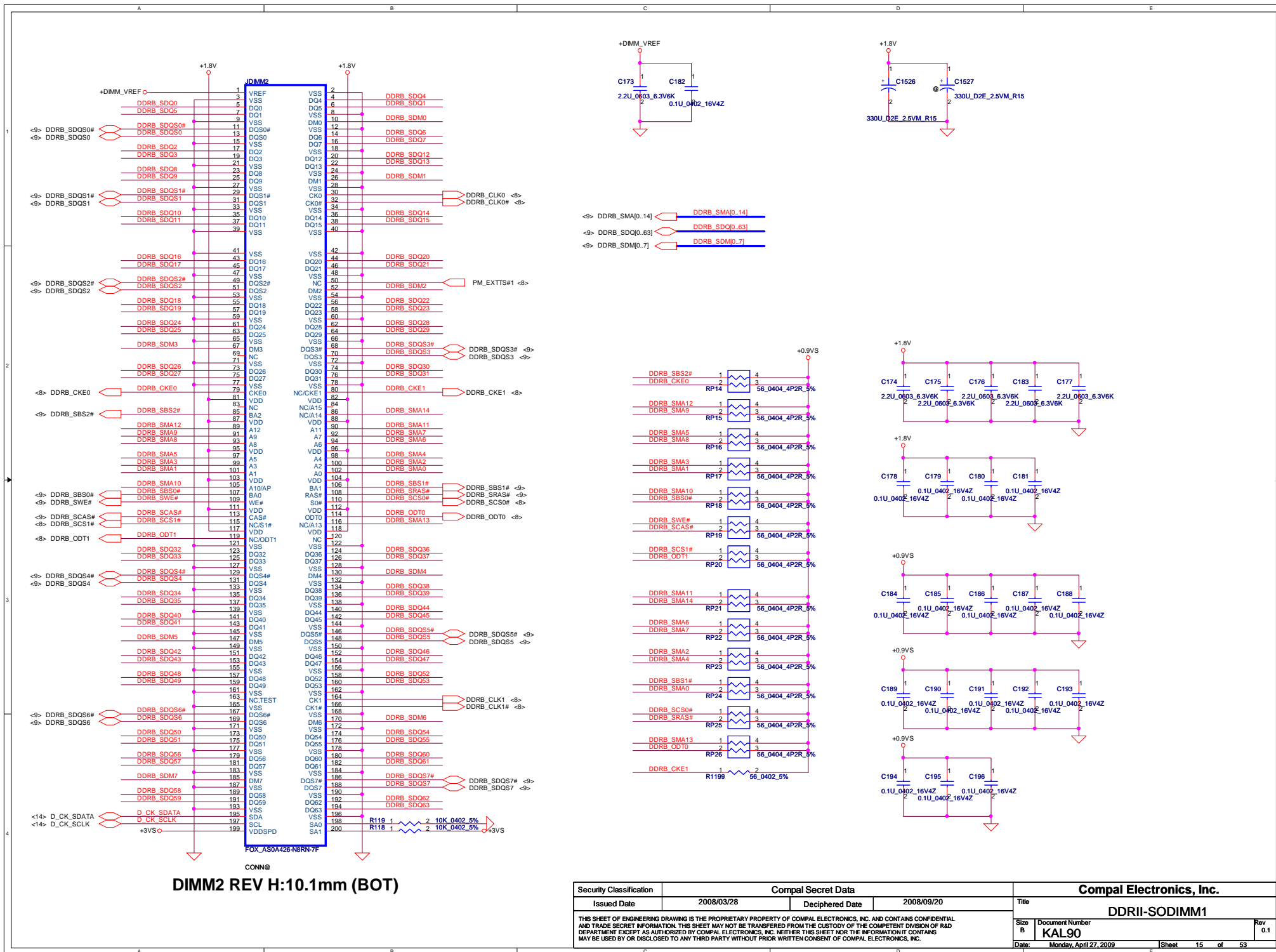












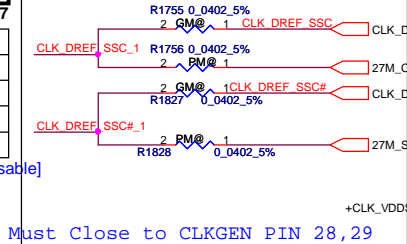
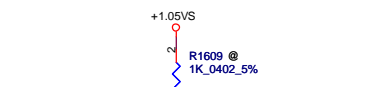
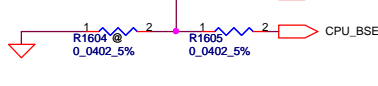
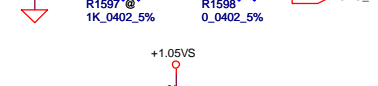
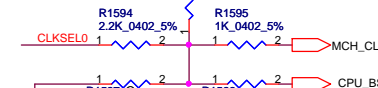
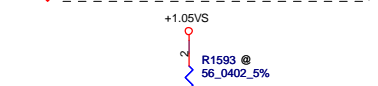
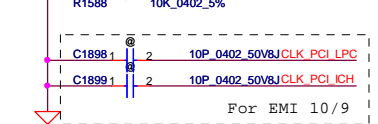
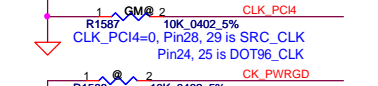
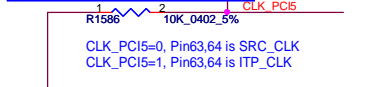
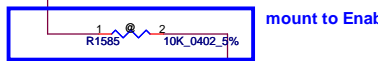
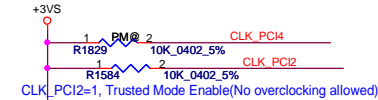
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2008/03/28	Deciphered Date	2008/09/20	Title	DDRII-SODIMM1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Document Number	0.1
				KAL90	
Date:	Monday, April 27, 2009	Sheet	15	of	53

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	0	266	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

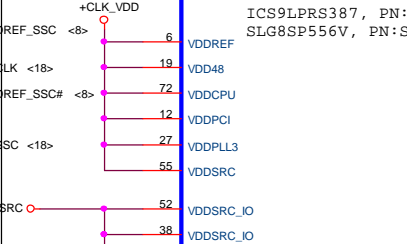
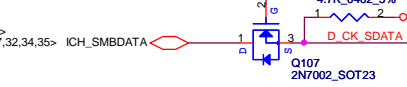
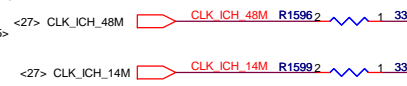
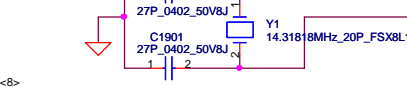
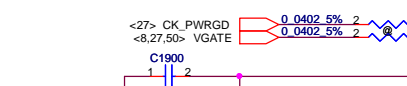
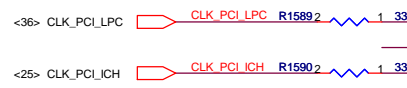
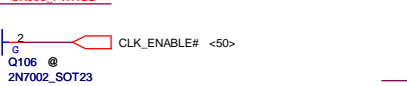
Table : ICS9LPRS387

CLK_REQ#	Control	Free-Run
CR#_10(WLAN)	PCIEX10	PCIEX0
CR#_6(MCH)	PCIEX6	PCIEX1
CR#_4(NEW CARD)	PCIEX4	
CR#_9(MINI CARDII)	PCIEX9	

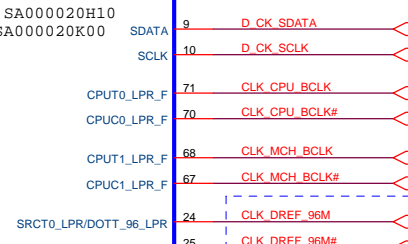
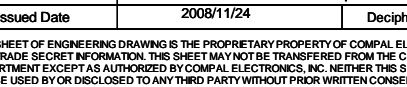
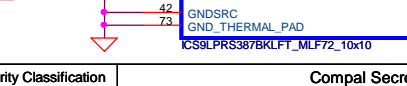
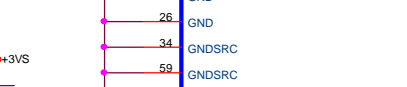
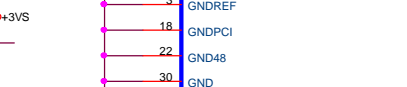
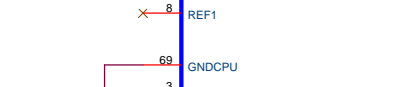
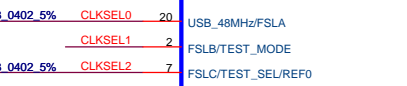
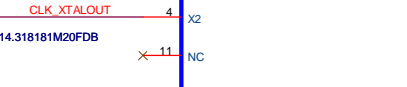
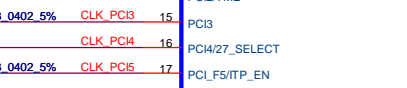
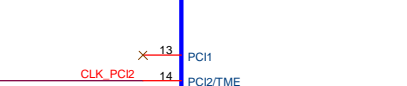
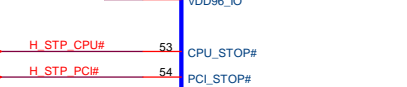
SRCT7(VGA\_CLK): Discrete VGA[Enable] UMA[Disable]



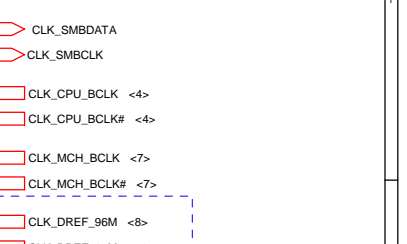
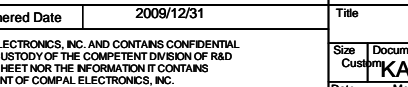
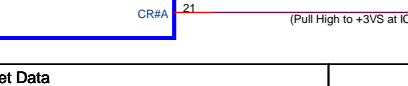
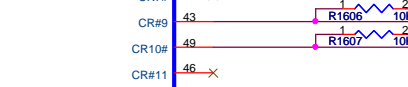
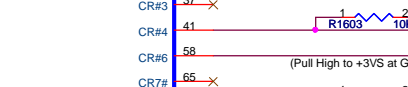
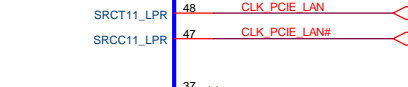
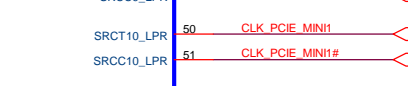
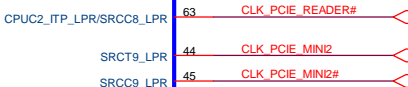
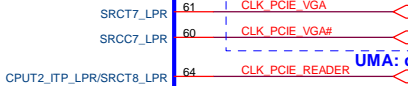
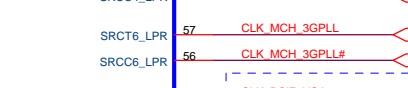
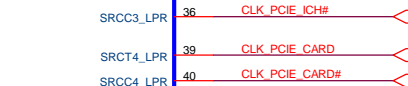
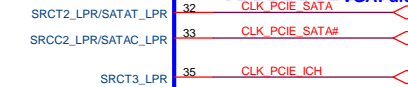
Must Close to CLKGEN PIN 28,29



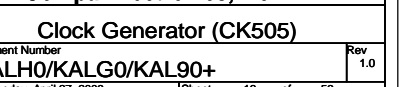
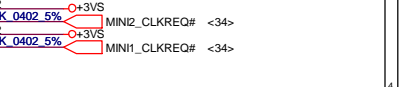
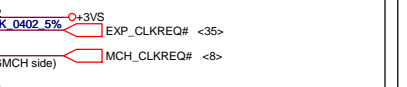
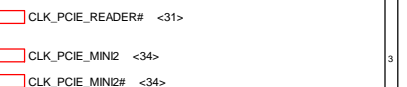
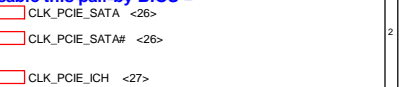
Must Close to CLKGEN PIN 28,29



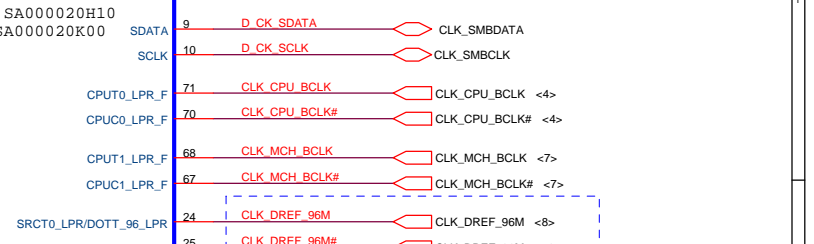
Must Close to CLKGEN PIN 28,29



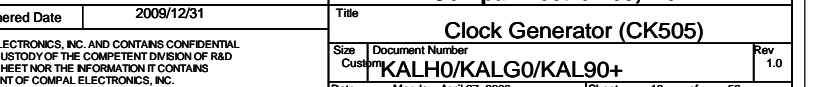
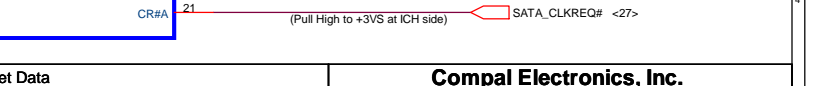
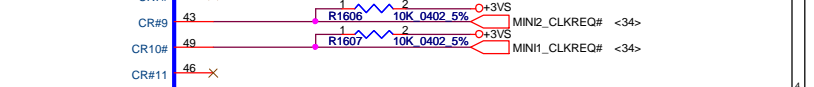
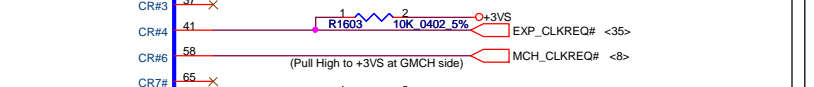
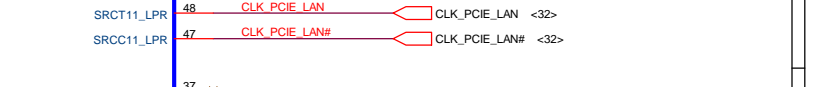
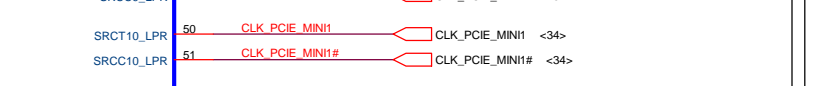
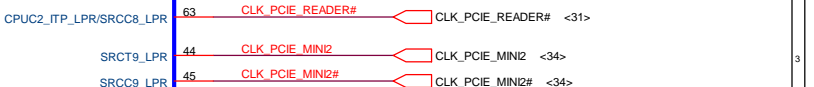
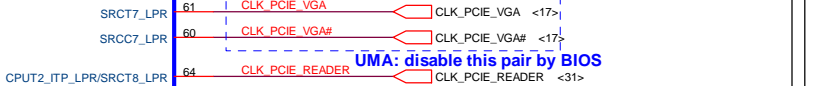
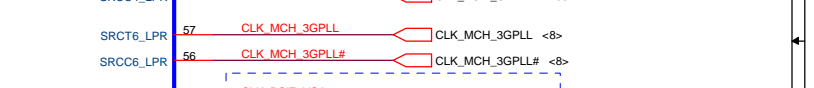
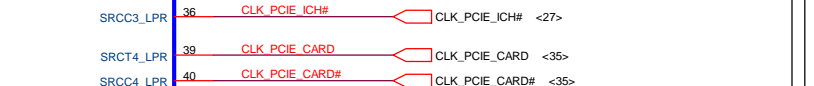
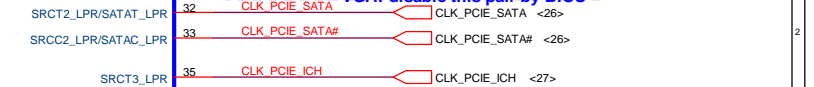
Must Close to CLKGEN PIN 28,29



## Clock Generator



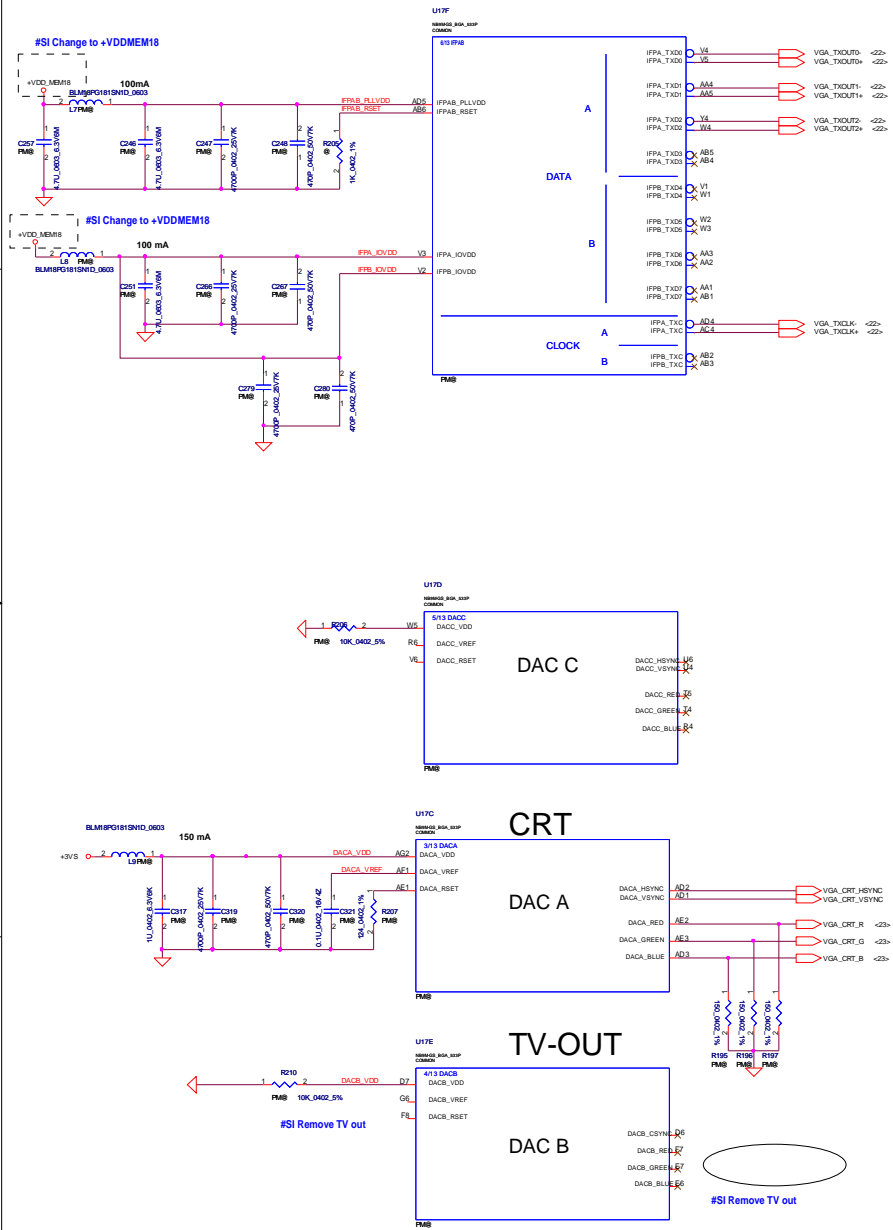
Must Close to CLKGEN PIN 28,29



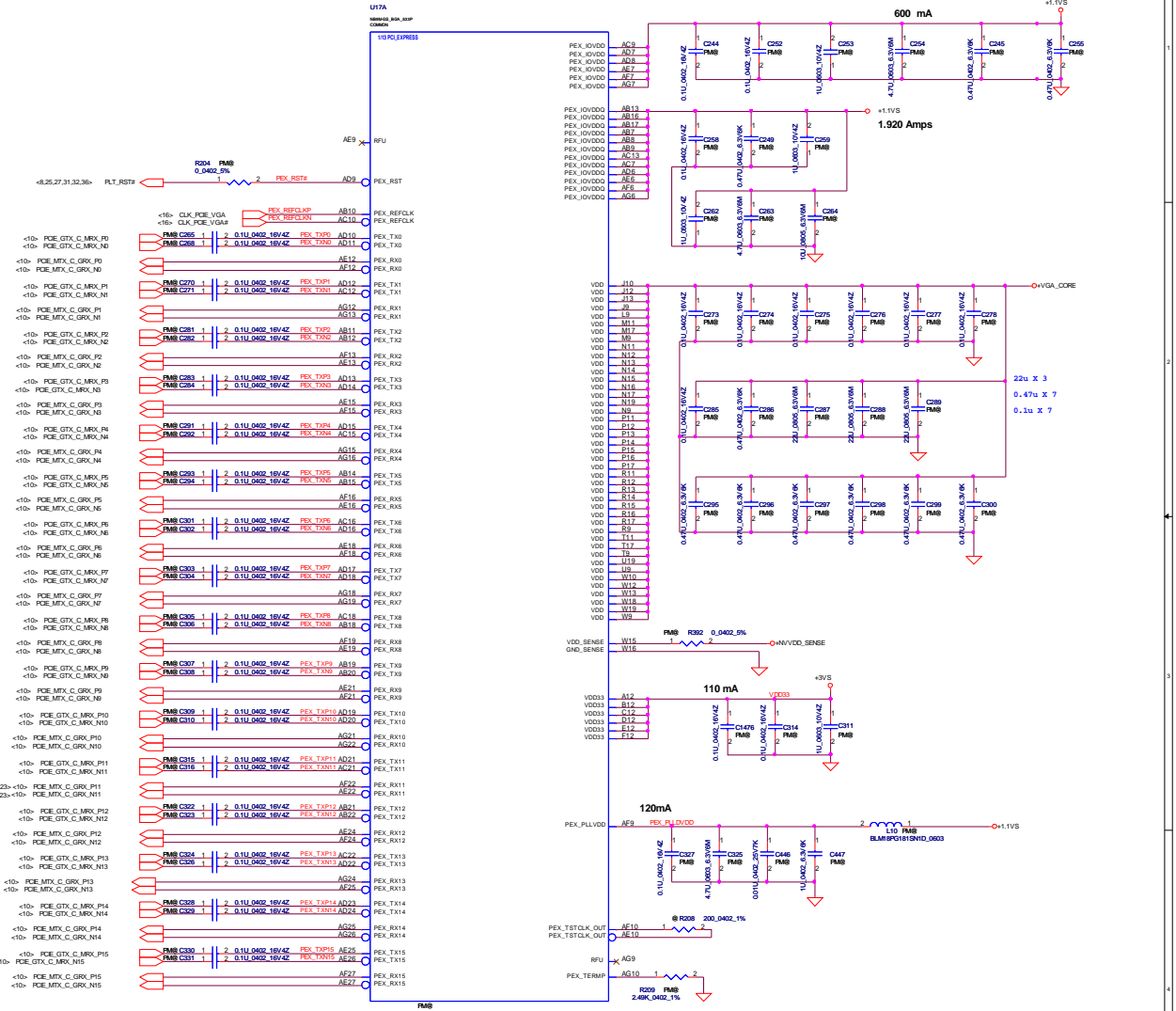
Security Classification		Compal Secret Data				Compal Electronics, Inc.				
Issued Date		2008/11/24		Deciphered Date		2009/12/31		Title		
								Clock Generator (CK505)		
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						Custom		KALH0/KALG0/KAL90+		
						Date:		Monday, April 27, 2009		



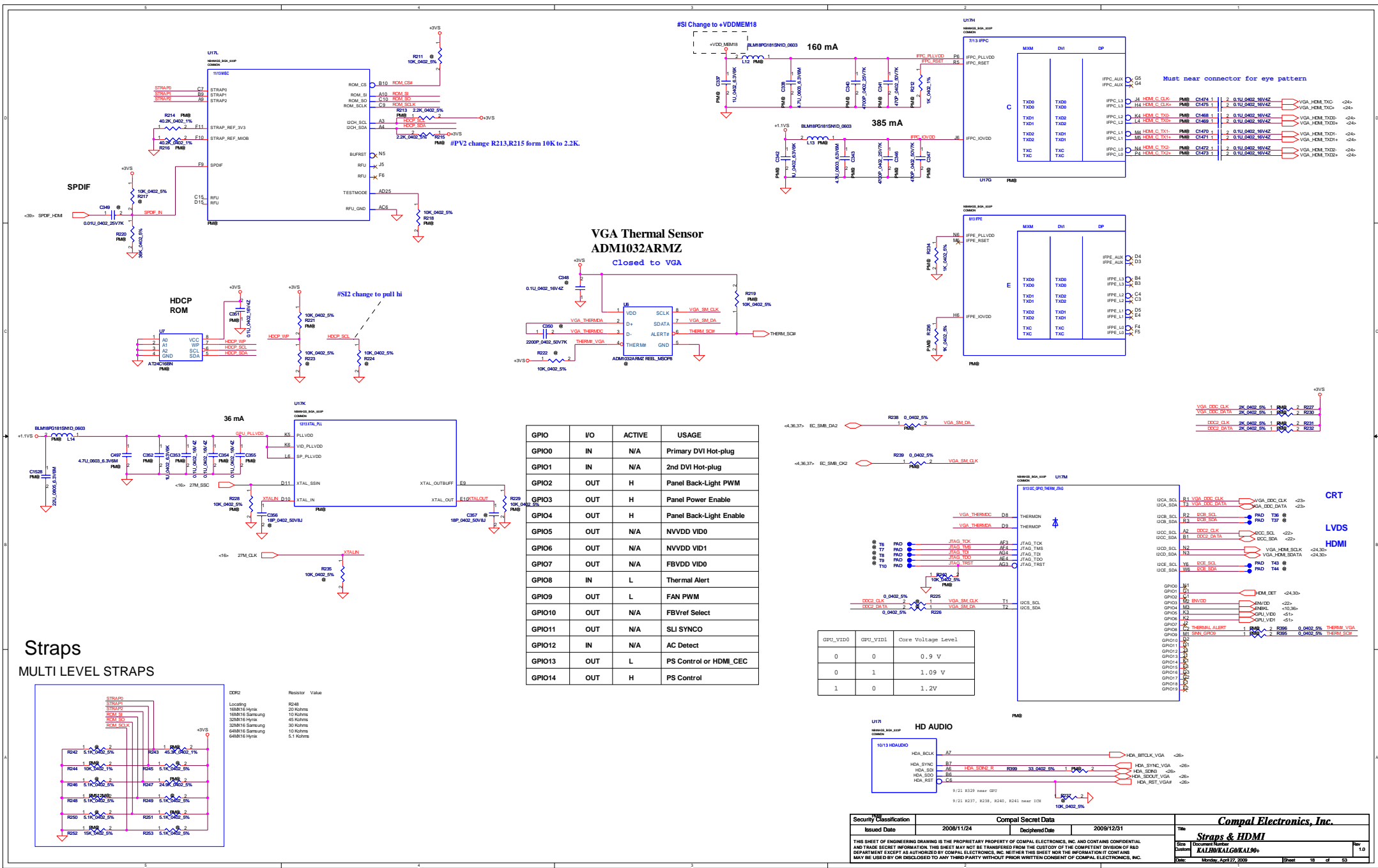
## LVDS & DAC Interface



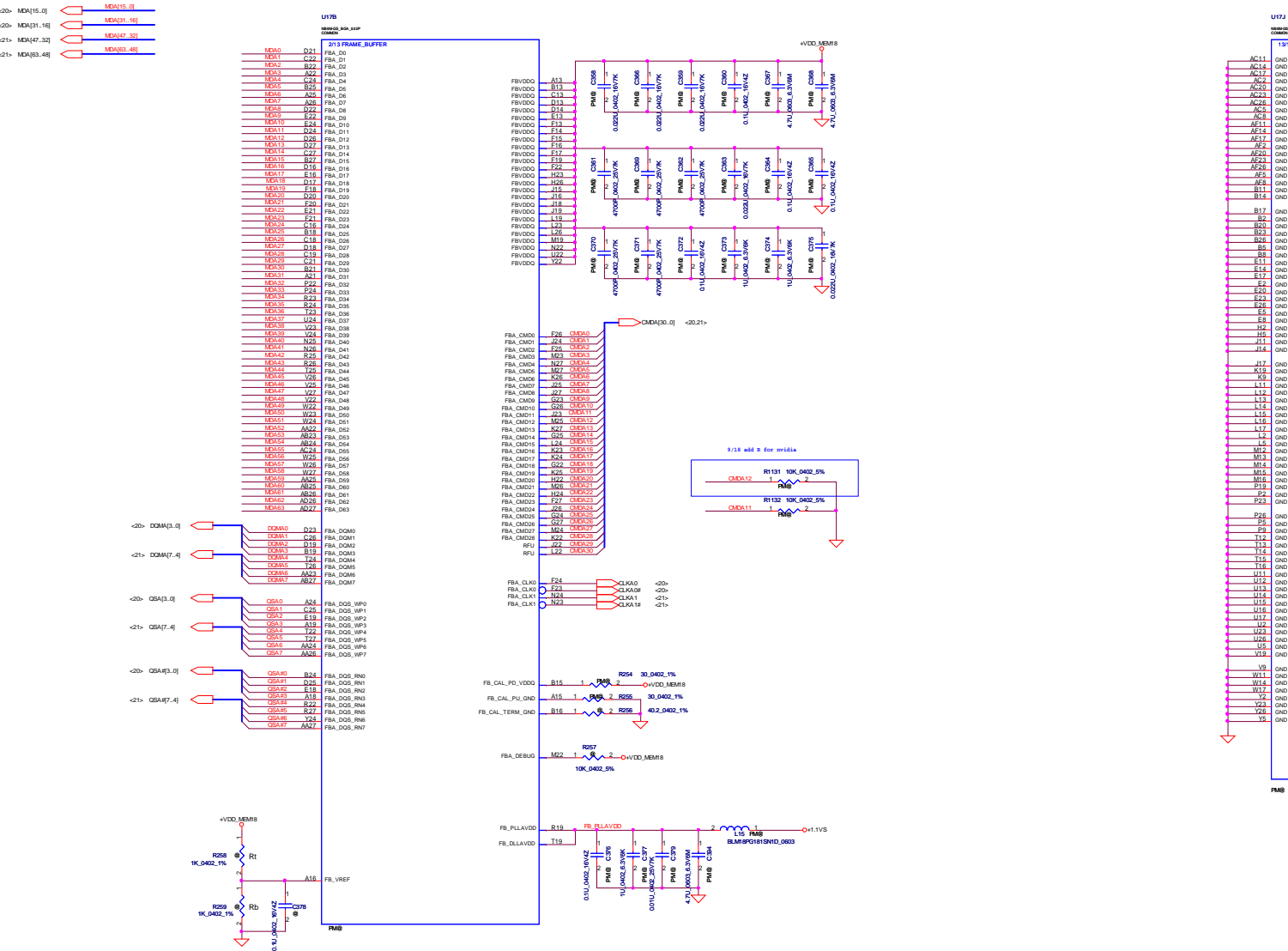
## PEG Interface



Security Classification	Compul Secret Data		Title	
Issued Date	2008/11/24	Deciphered Date	2009/12/51	Compul Electronics, Inc.
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			Size	Document Number
			Date	KALIN/KALGO/KAL9L
			Drawn	Monday, April 27, 2009
			Sheet	17 of 53



VRAM Interface



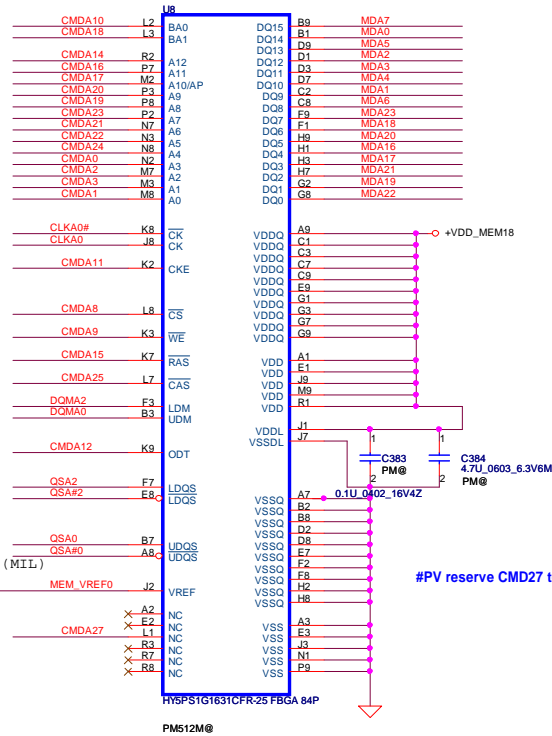
Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev	1.0
Doc	Rev	Rev	Rev	Rev	Rev

# VRAM DDR2 chips (256MB & 512MB)

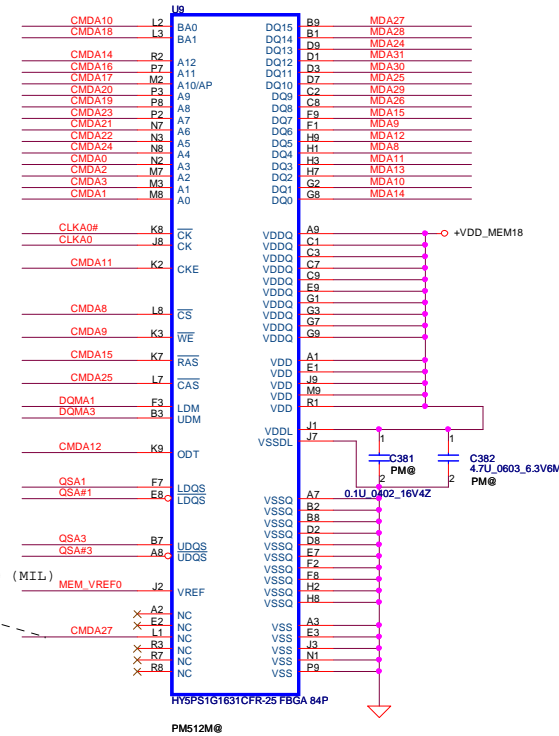
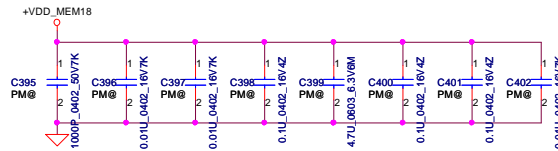
32Mx16 DDR2 400MHz \*4==>256MB

64Mx16 DDR2 400MHz\*4==>512MB

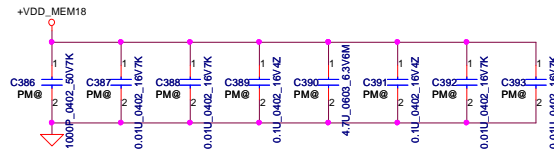
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 <19,21> QSA# [7..0] QSA# [7..0]  
 <19,21> DQMA[7..0] DQMA[7..0]  
 <19,21> MDA[63..0] MDA[63..0]  
 <19,21> CMDA[30..0] CMDA[30..0]



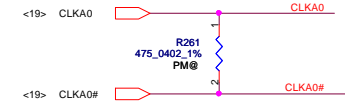
## DDR2 BGA MEMORY



## DDR BGA MEMORY

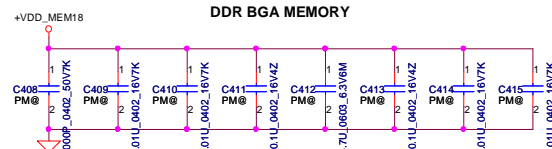
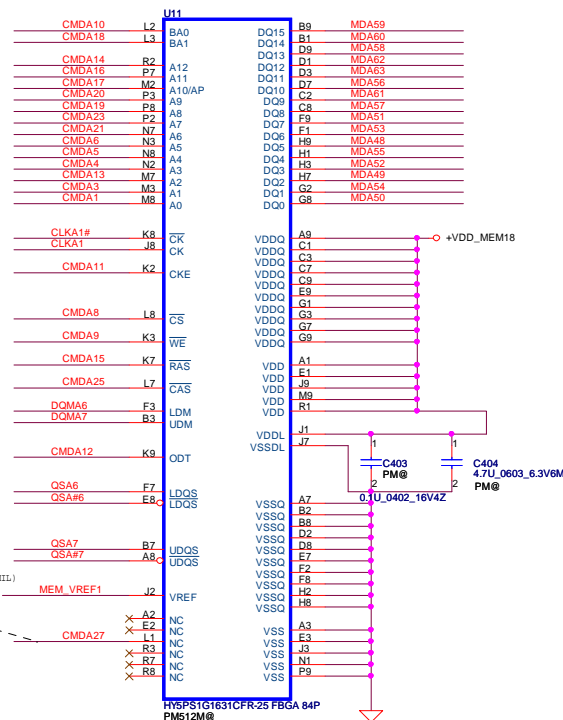
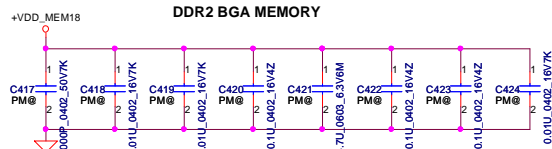
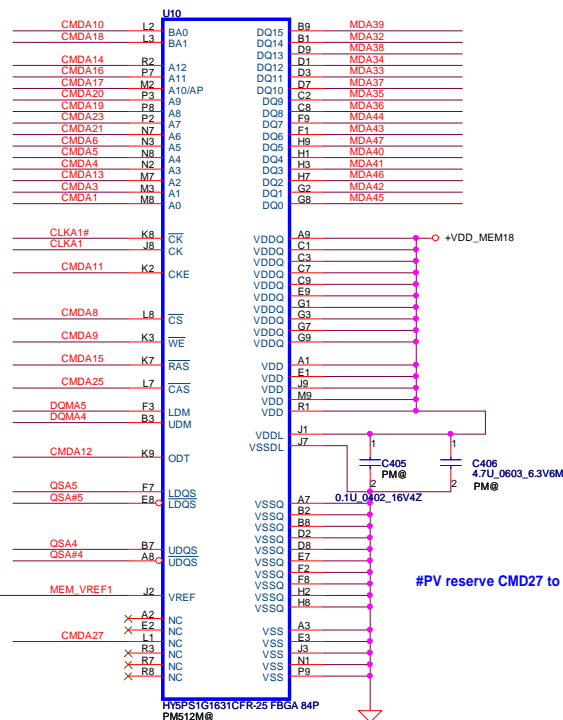
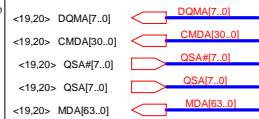


DATA Bus		
Address	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		

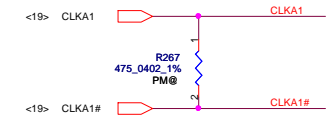


Security Classification		Compal Secret Data		Title	
Issued Date	2008/11/24	Deciphered Date	2009/12/31	VRAM 1	
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					KAL90
				Date	Monday, April 27, 2009
				Sheet	7 of 16

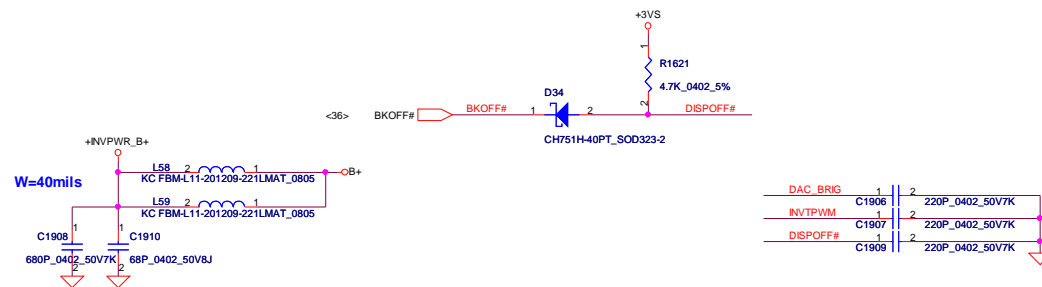
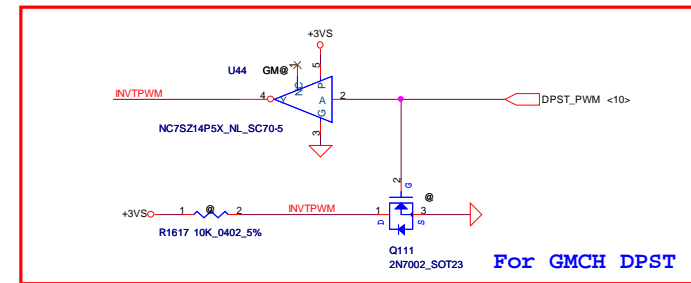
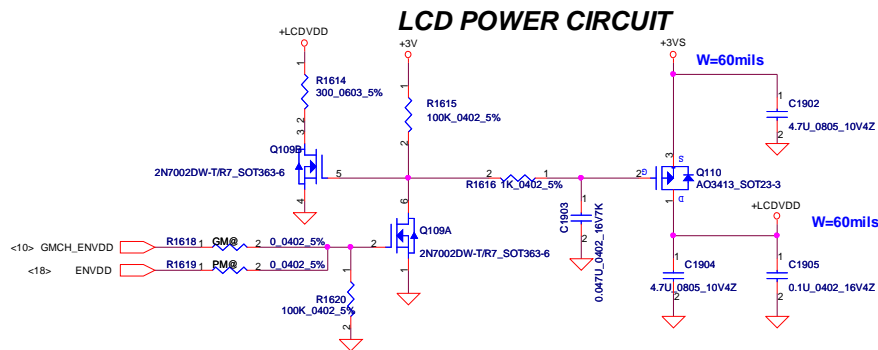
32Mx16 DDR2 400MHz \*4==>256MB  
64Mx16 DDR2 400MHz\*4==>512MB



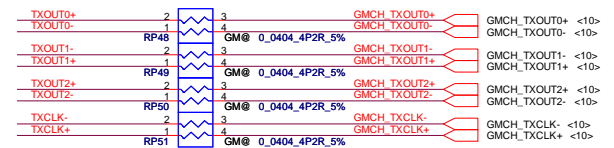
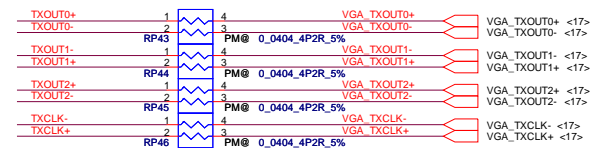
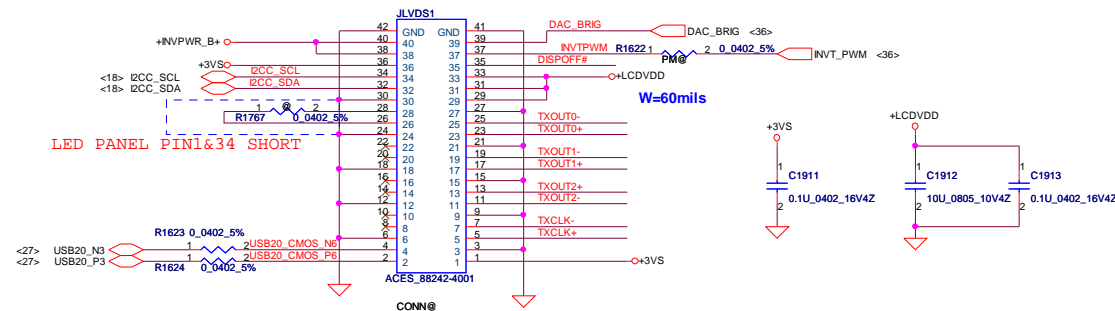
Address	DATA Bus	
	0..31	32..63
CMD0	A3	
CMD1	A0	A0
CMD2	A2	
CMD3	A1	A1
CMD4		A3
CMD5		A4
CMD6		A5
CMD7		
CMD8	CS#	CS#
CMD9	WE#	WE#
CMD10	BA0	BA0
CMD11	CKE	CKE
CMD12	ODT	ODT
CMD13		
CMD14	A12	A12
CMD15	RAS#	RAS#
CMD16	A11	A11
CMD17	A10	A10
CMD18	BA1	BA1
CMD19	A8	A8
CMD20	A9	A9
CMD21	A6	A6
CMD22	A5	
CMD23	A7	A7
CMD24	A4	
CMD25	CAS#	CAS#
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		
CMD29		
CMD30		



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Issued Date	2008/11/24	Deciphered Date	2009/12/31	Title	VRAM 2
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				KAL90	
				Date:	Monday, April 27, 2009
				Sheet	8 of 16

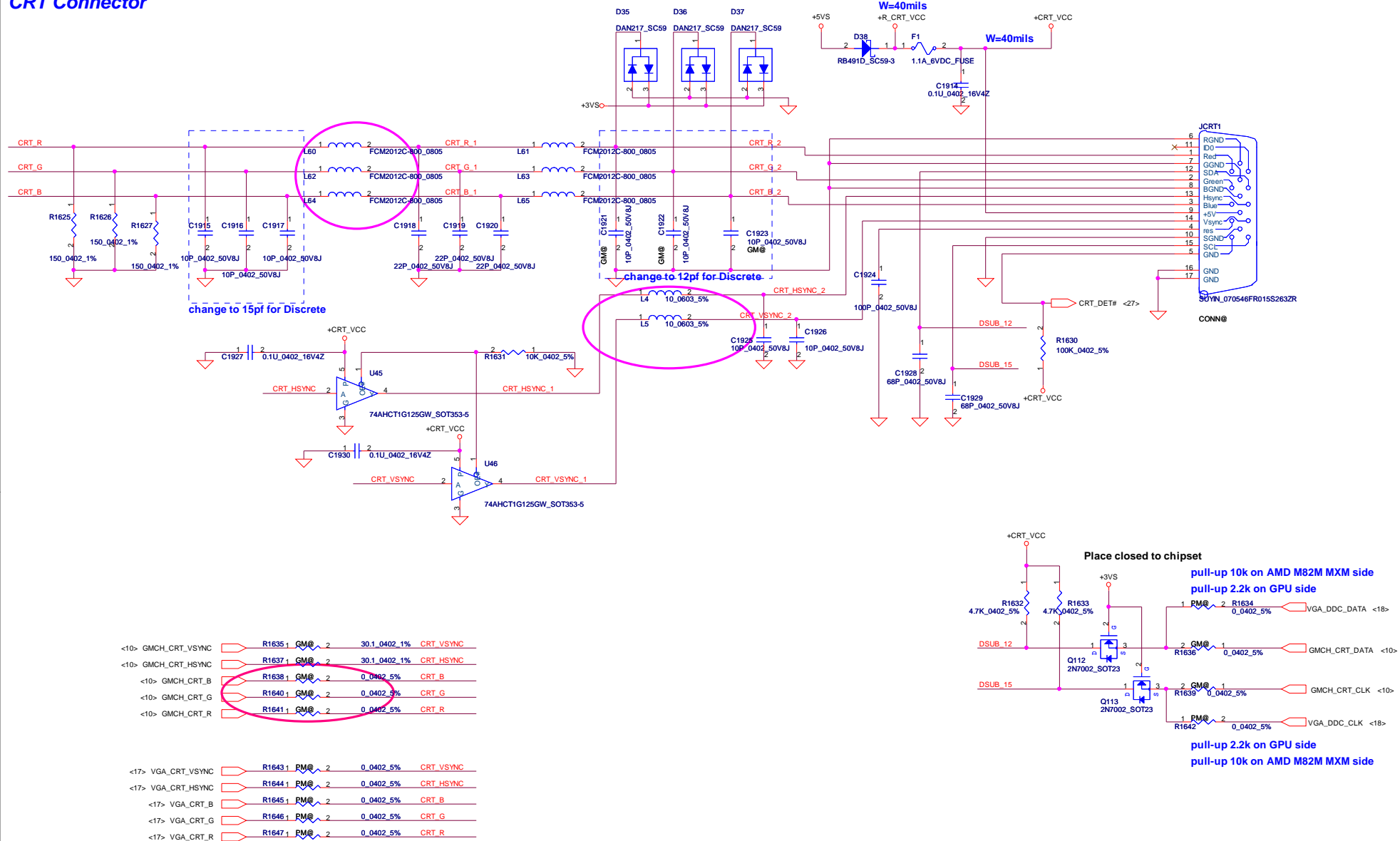


**LCD/PANEL BD. Conn.**

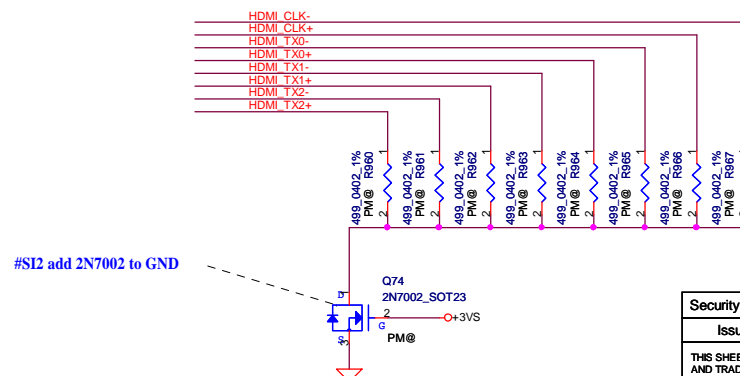
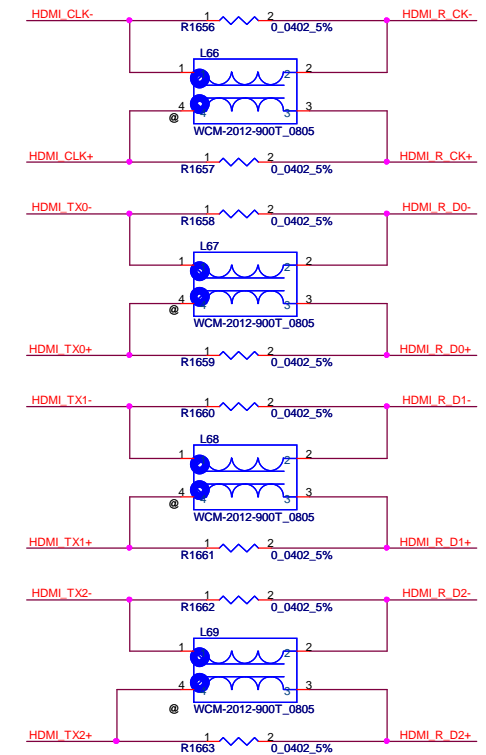
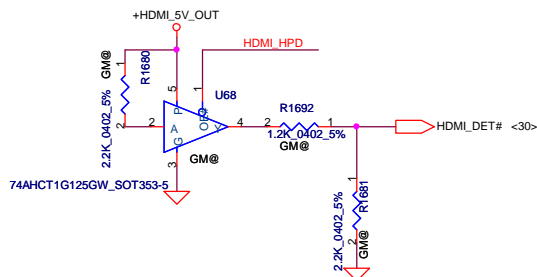
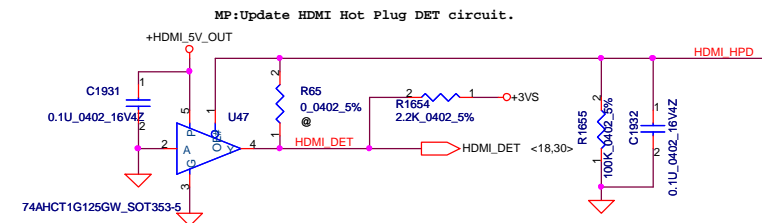
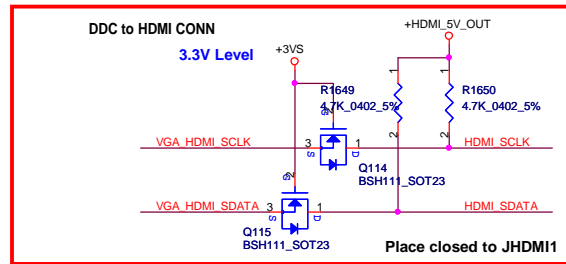


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Size		Document Number		Rev	
Customer		KALHO/KALGO/KAL90+		1.0	
Date		Monday, April 27, 2009		Sheet 22 of 53	

# CRT Connector

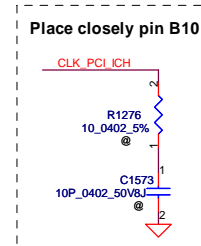
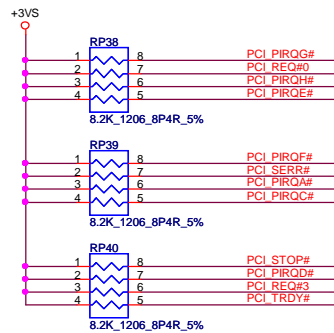


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Size	B	Document Number	KALHO/KALGO/KAL90+		Rev
Date	Monday, April 27, 2009	Sheet	23	of	53

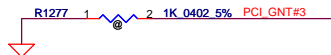


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				Customer	KALHO/KALGO/KAL90+		1.0
				Date:	Monday, April 27, 2009	Sheet	24 of 53

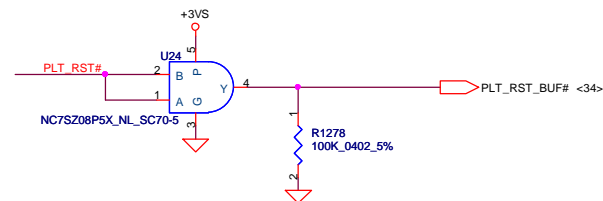
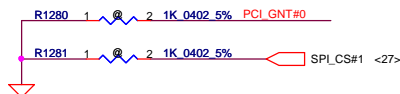




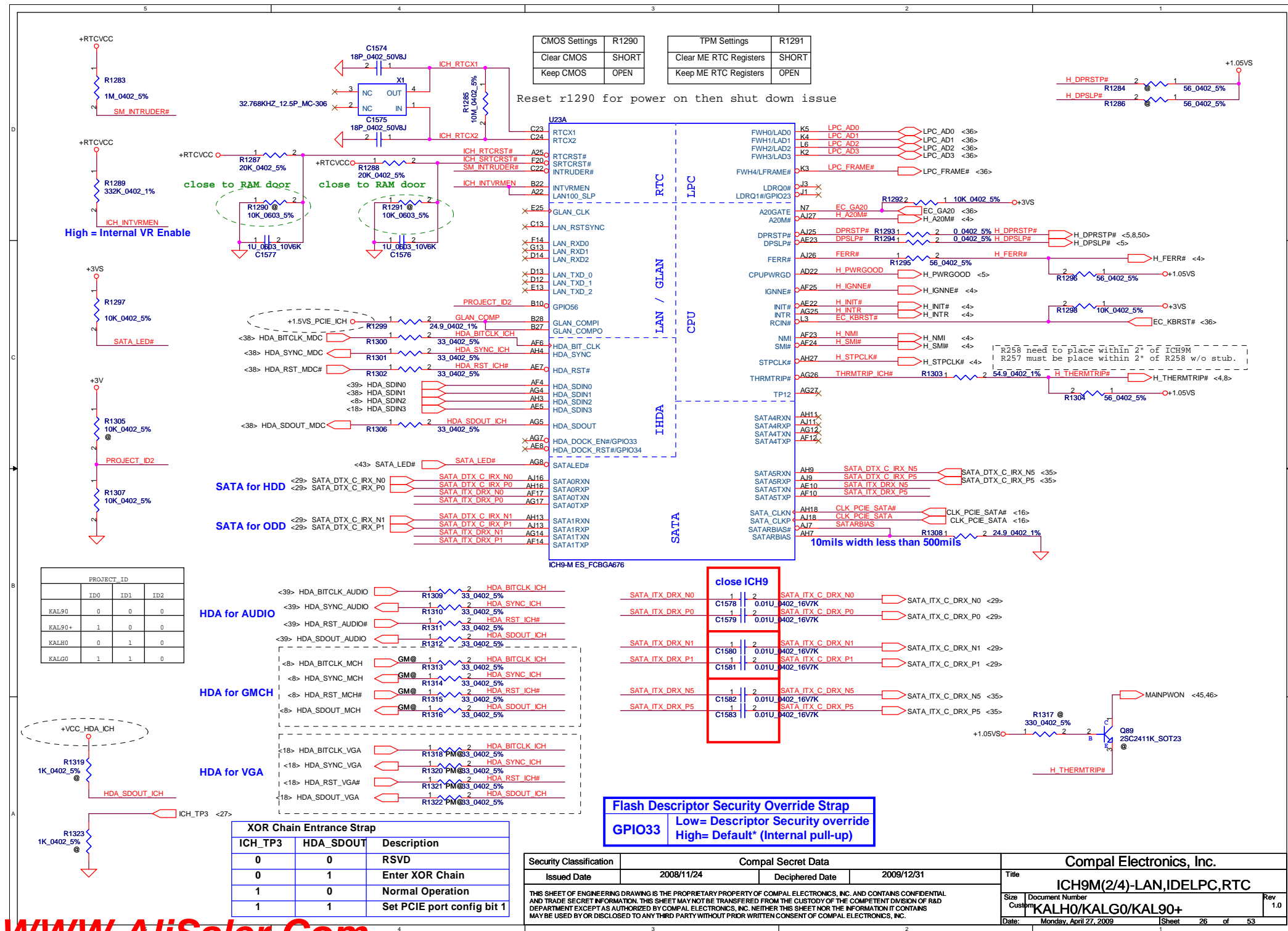
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*



Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*



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					KALH0/KALG0/KAL90+	1.0		
				Date:	Monday, April 27, 2009	Sheet	25 of 53	

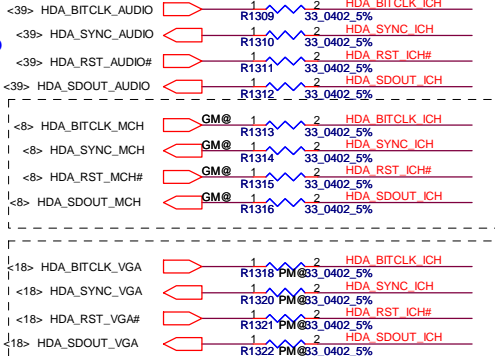


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ID0	ID1	ID2	
KAL90	0	0	0
KAL90+	1	0	0
KALH0	0	1	0
KALG0	1	1	0

HDA for AUDIO

HDA for GMCH

HDA for VGA

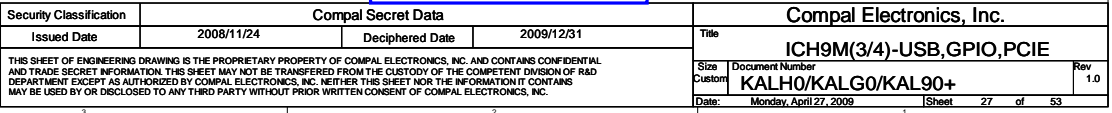


Flash Descriptor Security Override Strap  
GPIO33 Low= Descriptor Security override  
High= Default\* (Internal pull-up)

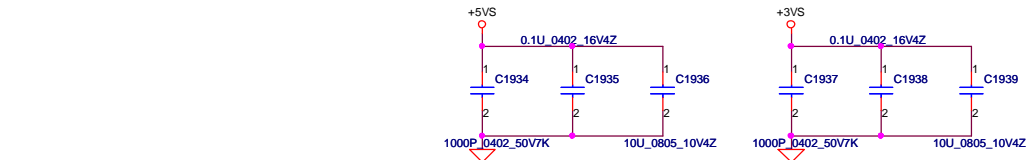
XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIe port config bit 1

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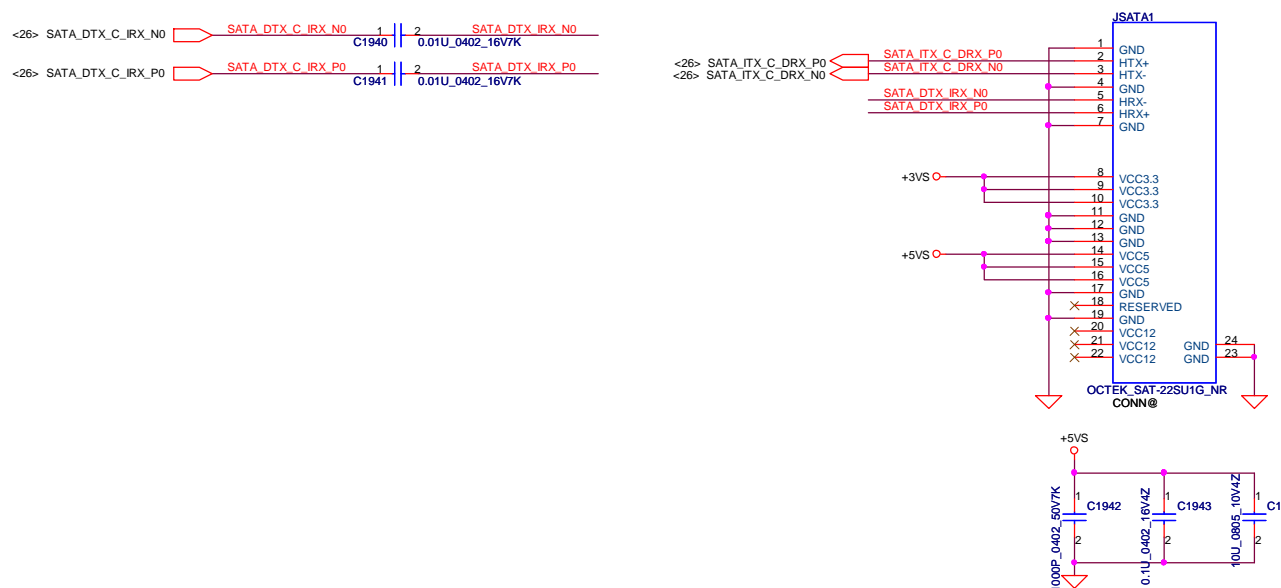
Compal Electronics, Inc.			
Title			
ICH9M(2/4)-LAN, IDE/LPC, RTC			
Size	Document Number	Rev	
Custom	KALH0/KALG0/KAL90+	1.0	
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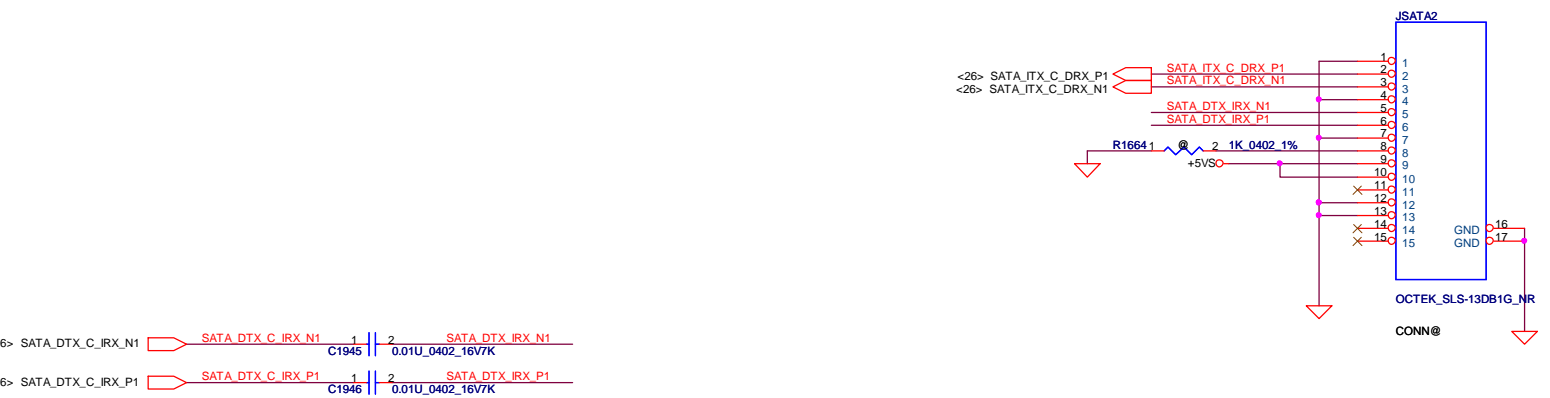




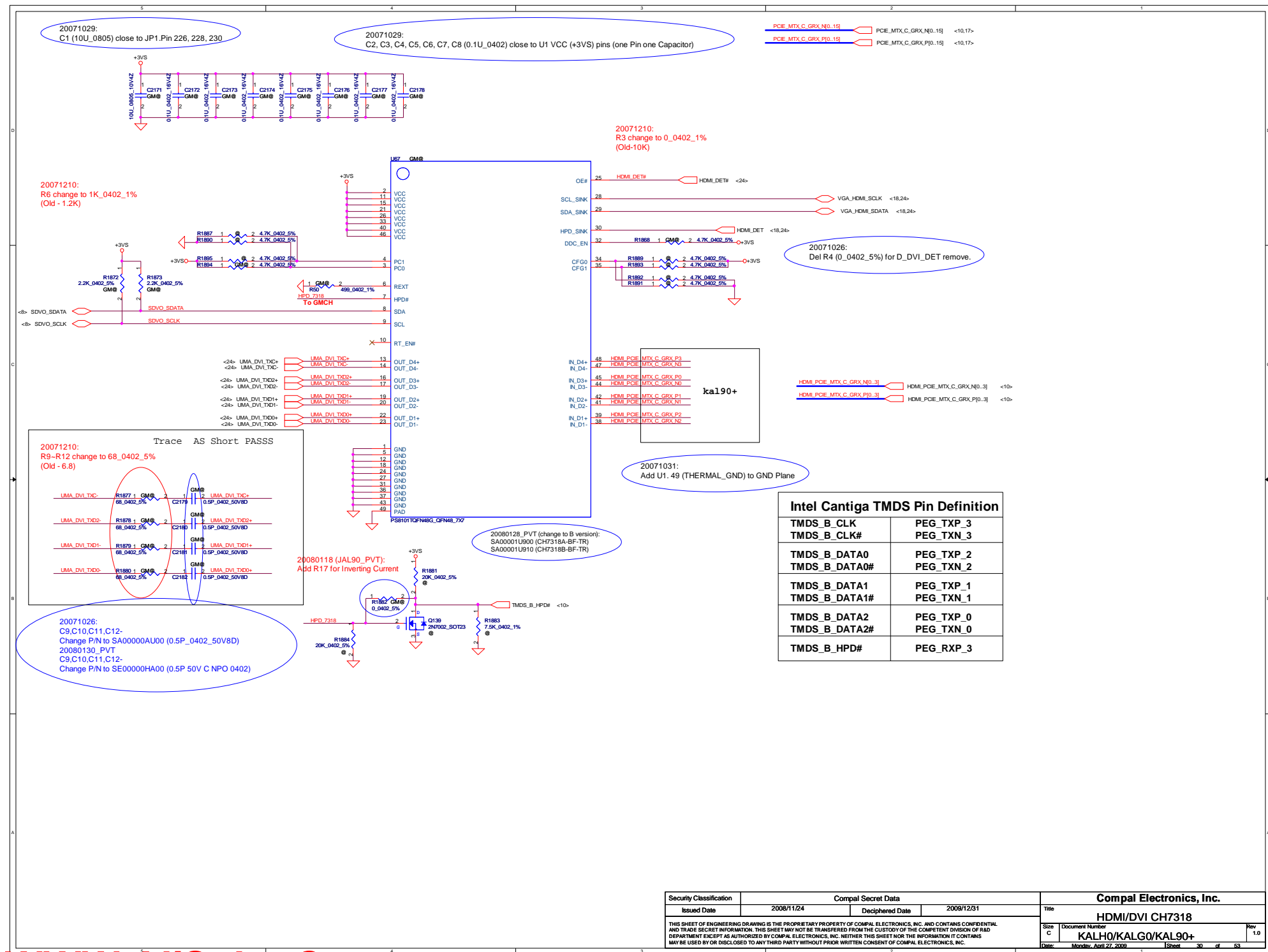
### SATA HDD Conn.



### SATA ODD Conn.

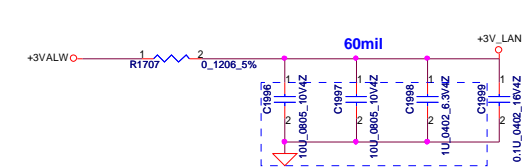


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								Size Custom	
		KALH0/KALG0/KAL90+		1.0					
Date:		Monday, April 27, 2009				Sheet		29 of 53	

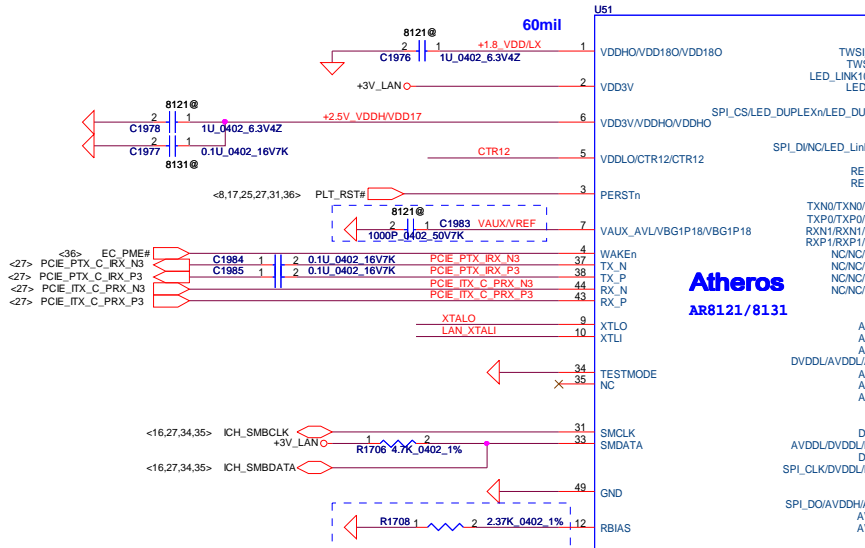
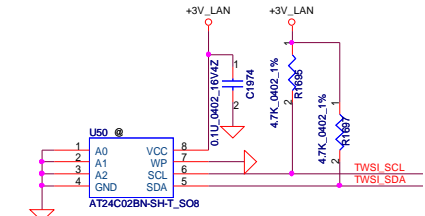
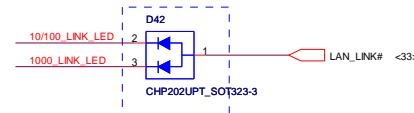
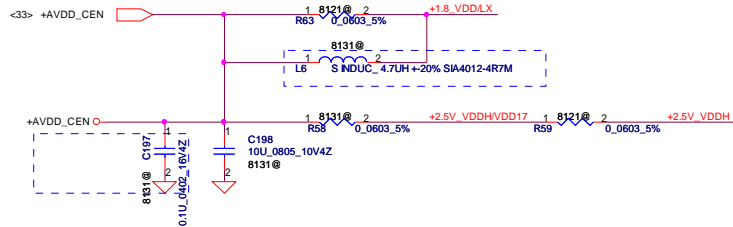
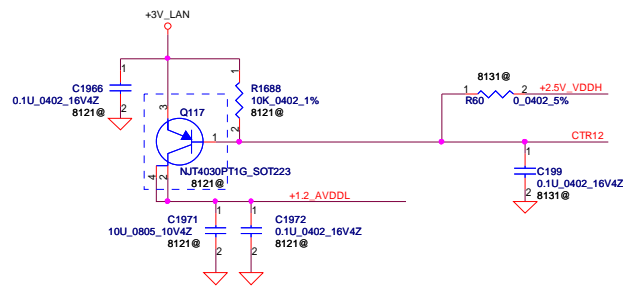








Place Close to Pin 2

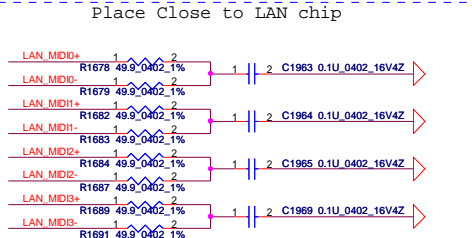


**Atheros**  
AR8121/8131

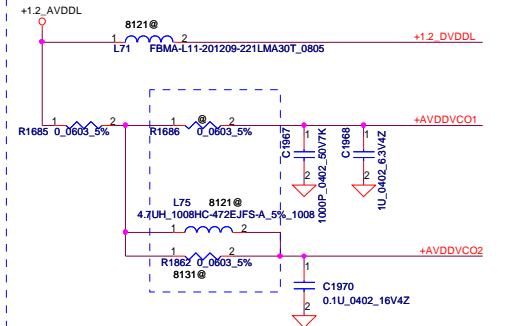
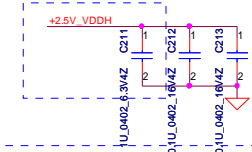
AR8121-AL1E\_QFN48\_6X6  
SA000031Z00 S IC AR8131-AL1E QFN 48P E-LAN CTRL  
8121@  
SA000025M00 S IC AR8121-AL1E QFN 48P E-LAN CTRL

Place Close to Pin 28、32、45、46  
C1750 and C1730 close to Pin46  
C1072 close to Pin45

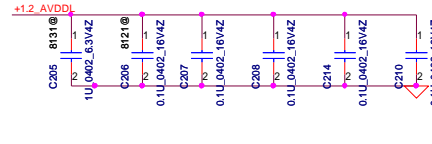
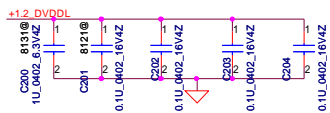
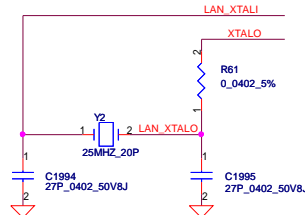
Place Close to Pin8、16、22、36、39  
C1066 and C1067 close to Pin8



Place Close to Pin15、19、25  
C1061 close to Pin15



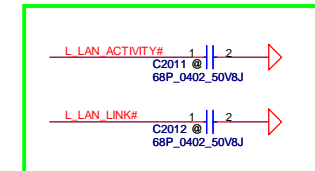
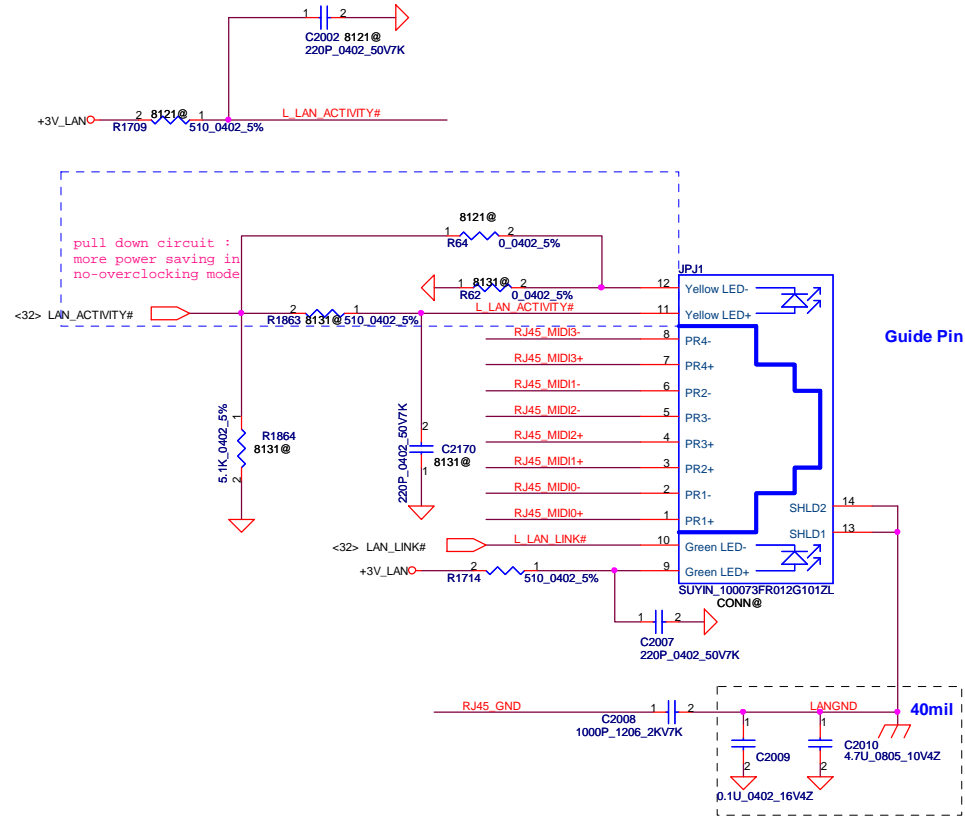
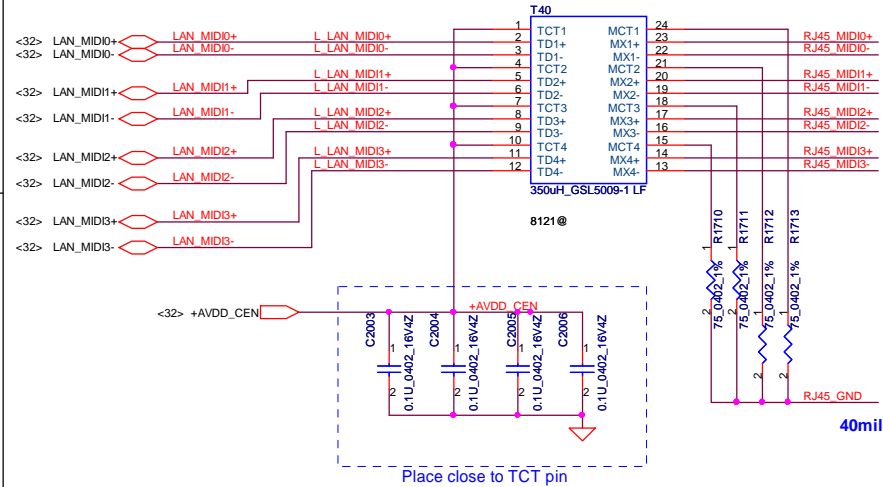
8121 If not overclocking , R1685 & L75 stuffed and R1686 & R1687 removed  
8131 If not overclocking , R1685 & R1682 stuffed and R1686 & L75 removed



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				Date	Monday, April 27, 2009
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# LAN AR8121/8112



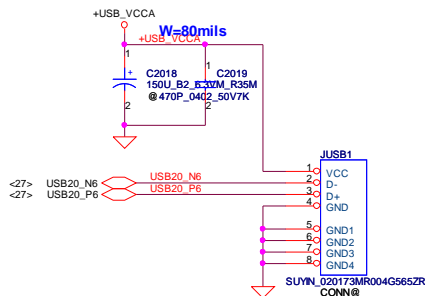
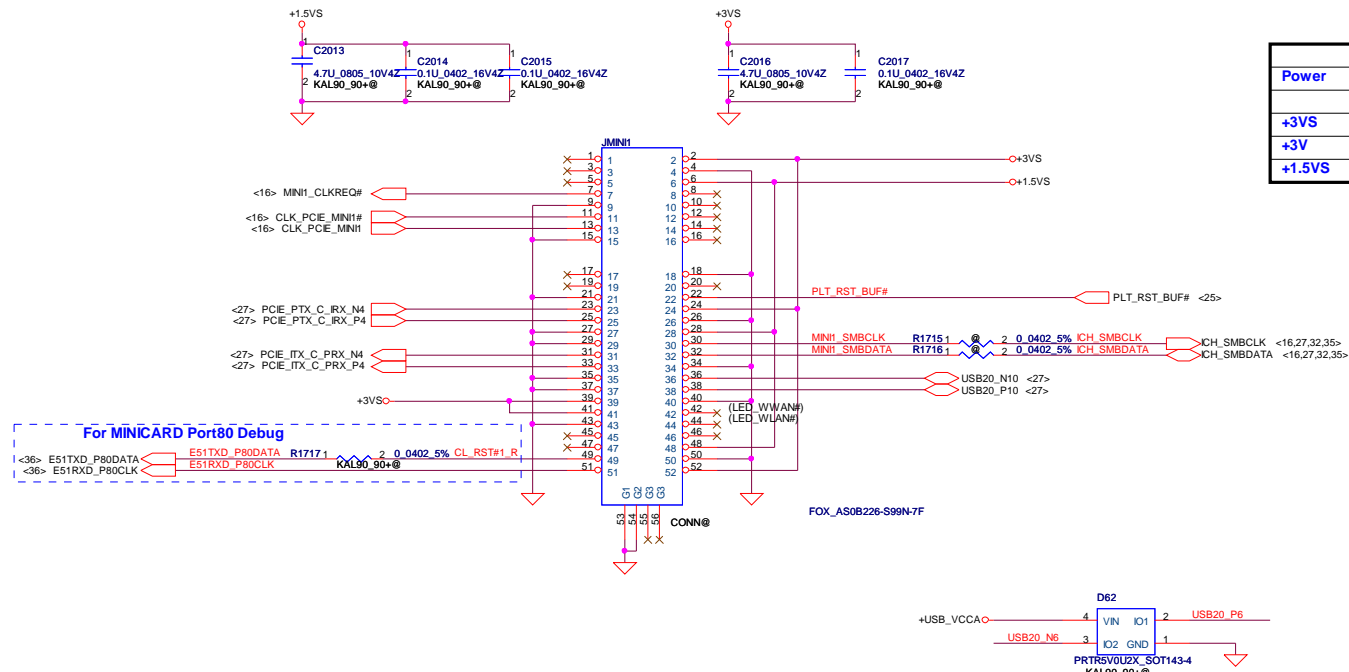
For EMI

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Size B	Document Number	KALH0/KALG0/KAL90+		Rev 1.0	
Date:	Monday, April 27, 2009	Sheet	33	of 53	

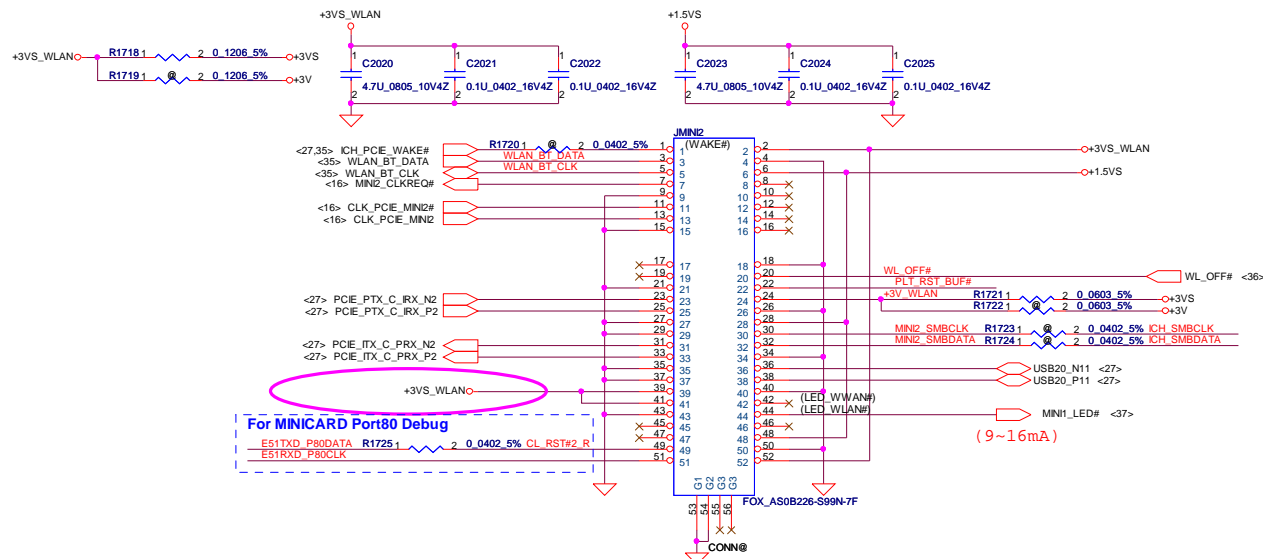
## For Robson2

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

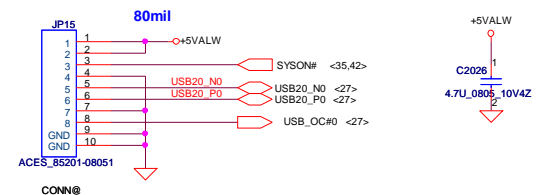
## USB CONN.



## For Wireless LAN

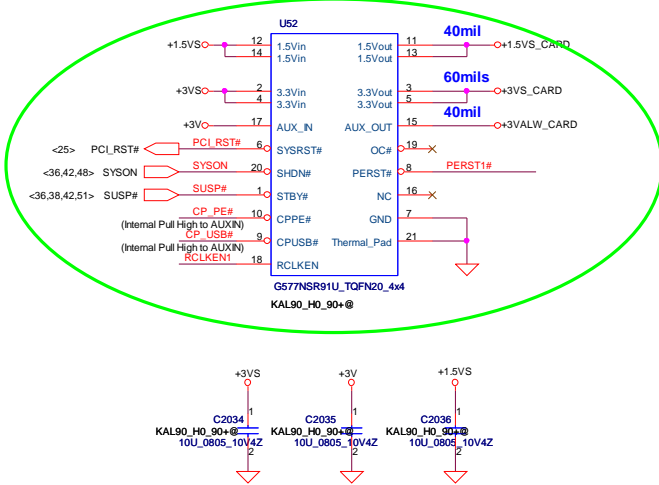


## To USB/B Connector

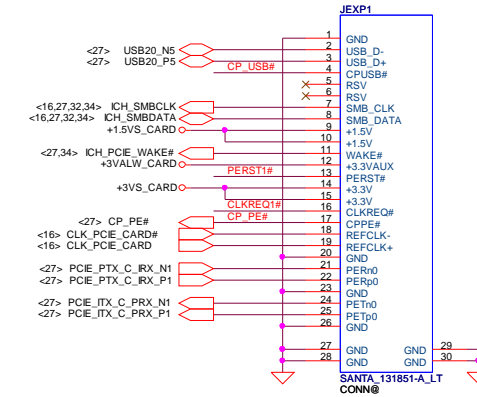


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Size B	Document Number	KALHO/KALGO/KAL90+		Date	Monday, April 27, 2009
		Sheet	34	of	53

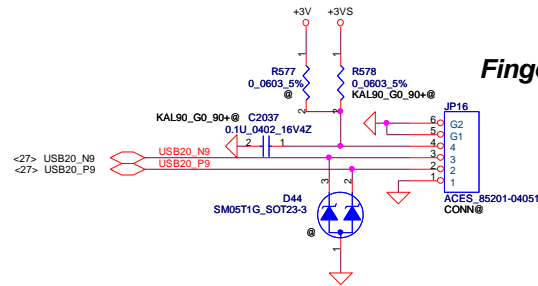
## New Card Power Switch



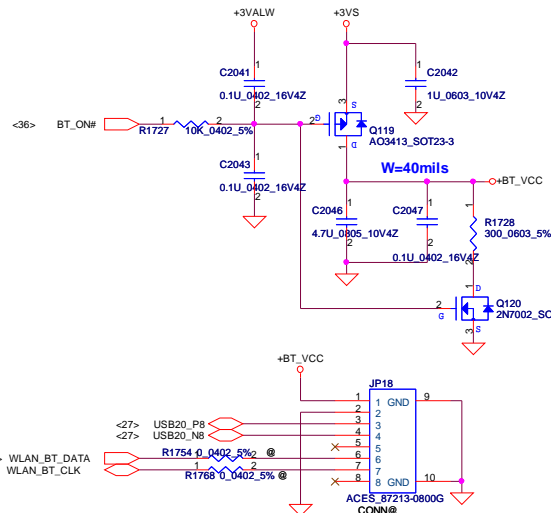
## New Card Socket (Left/TOP)



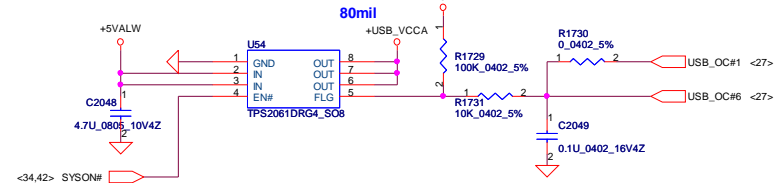
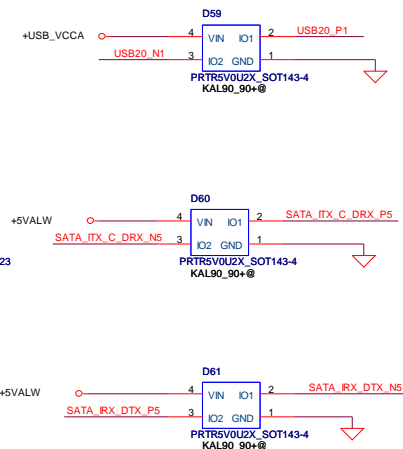
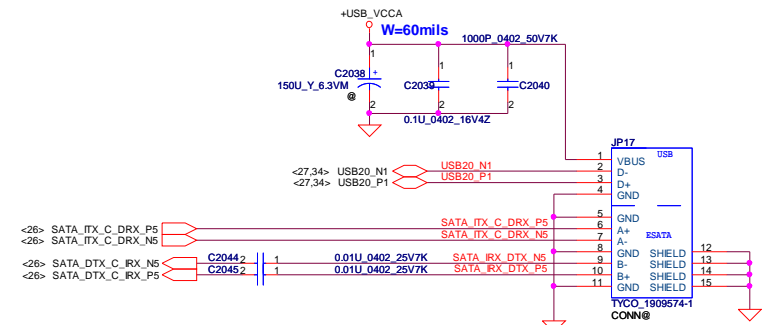
## Finger Print Conn.



## Bluetooth Conn.

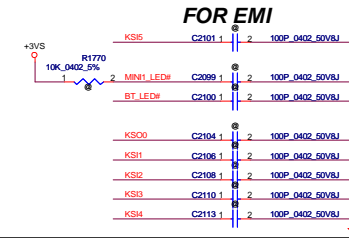
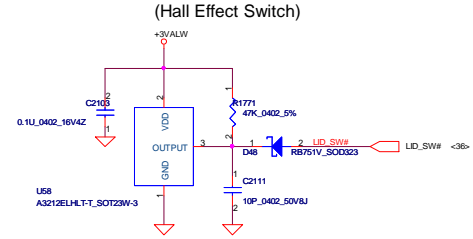
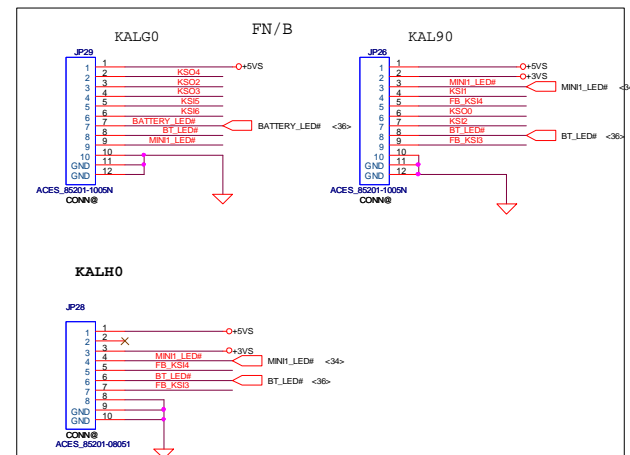
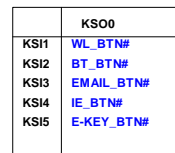
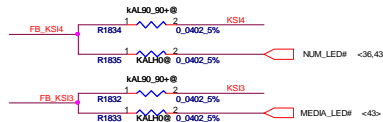
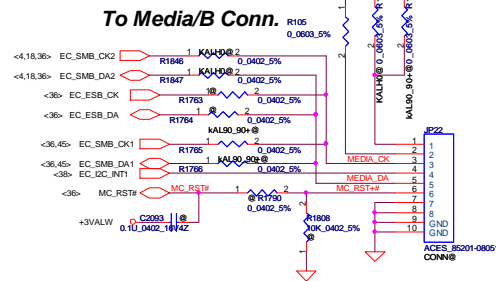
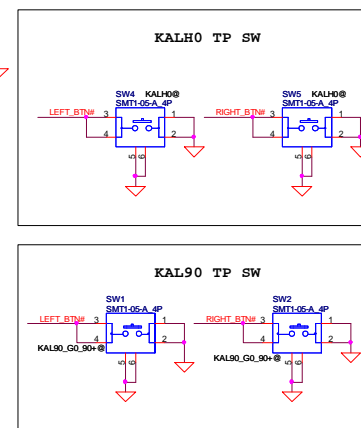
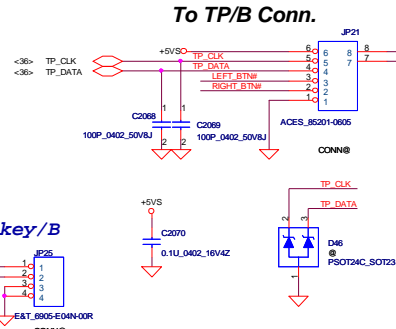


## ESATA CONN



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Size B	Document Number	KALHO/KALGO/KAL90+		Rev	1.0
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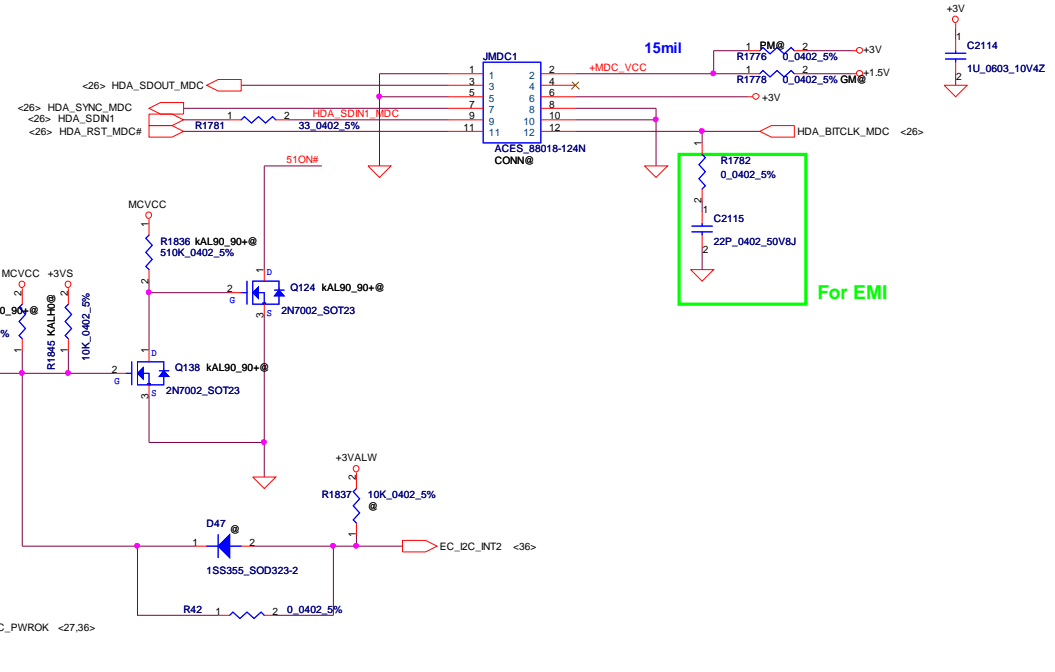
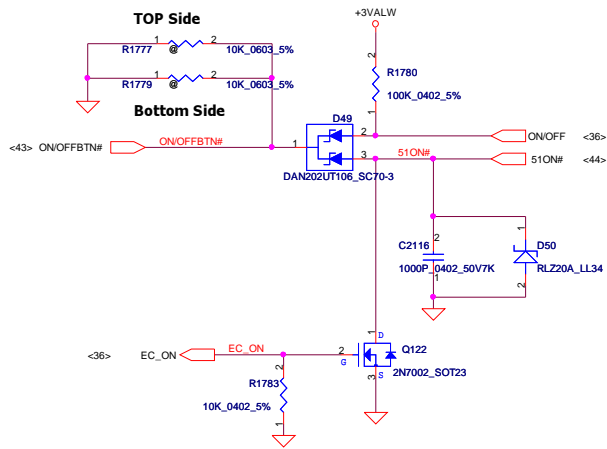


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				BIOS, I/O Port & K/B Connector					
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						Moder	Apr 22, 2009	Sheet	37

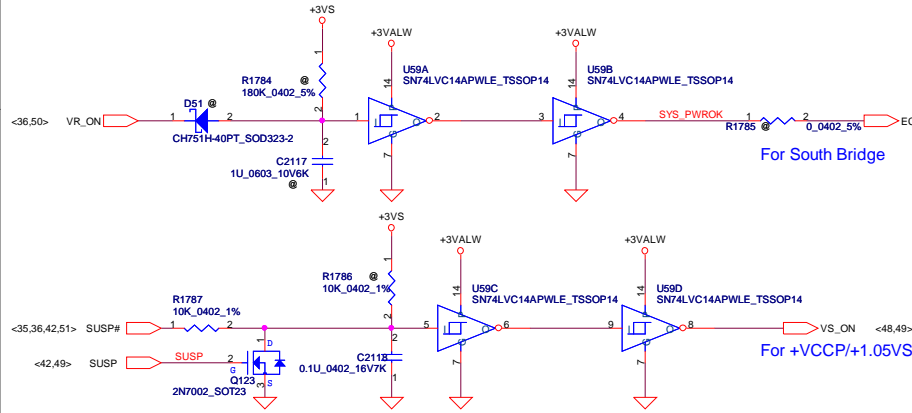
ON/OFF switch

## Power Button

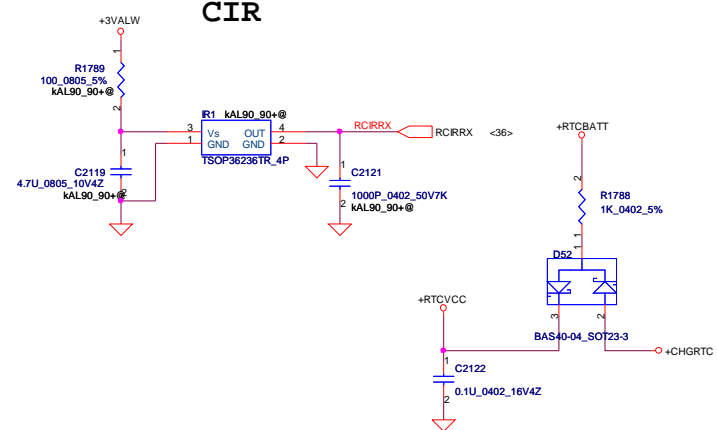
## HDA MDC Conn.



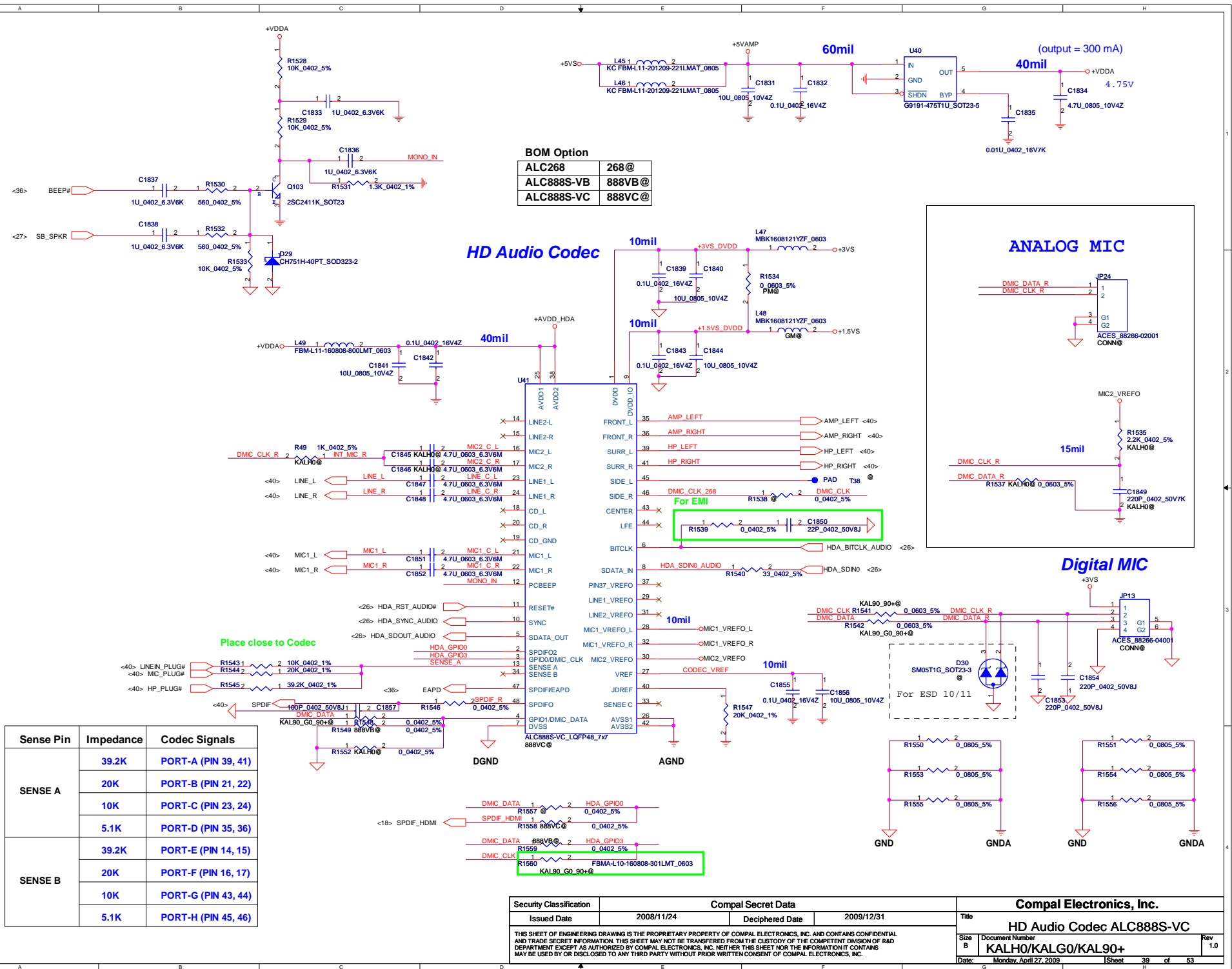
## Power ON Circuit

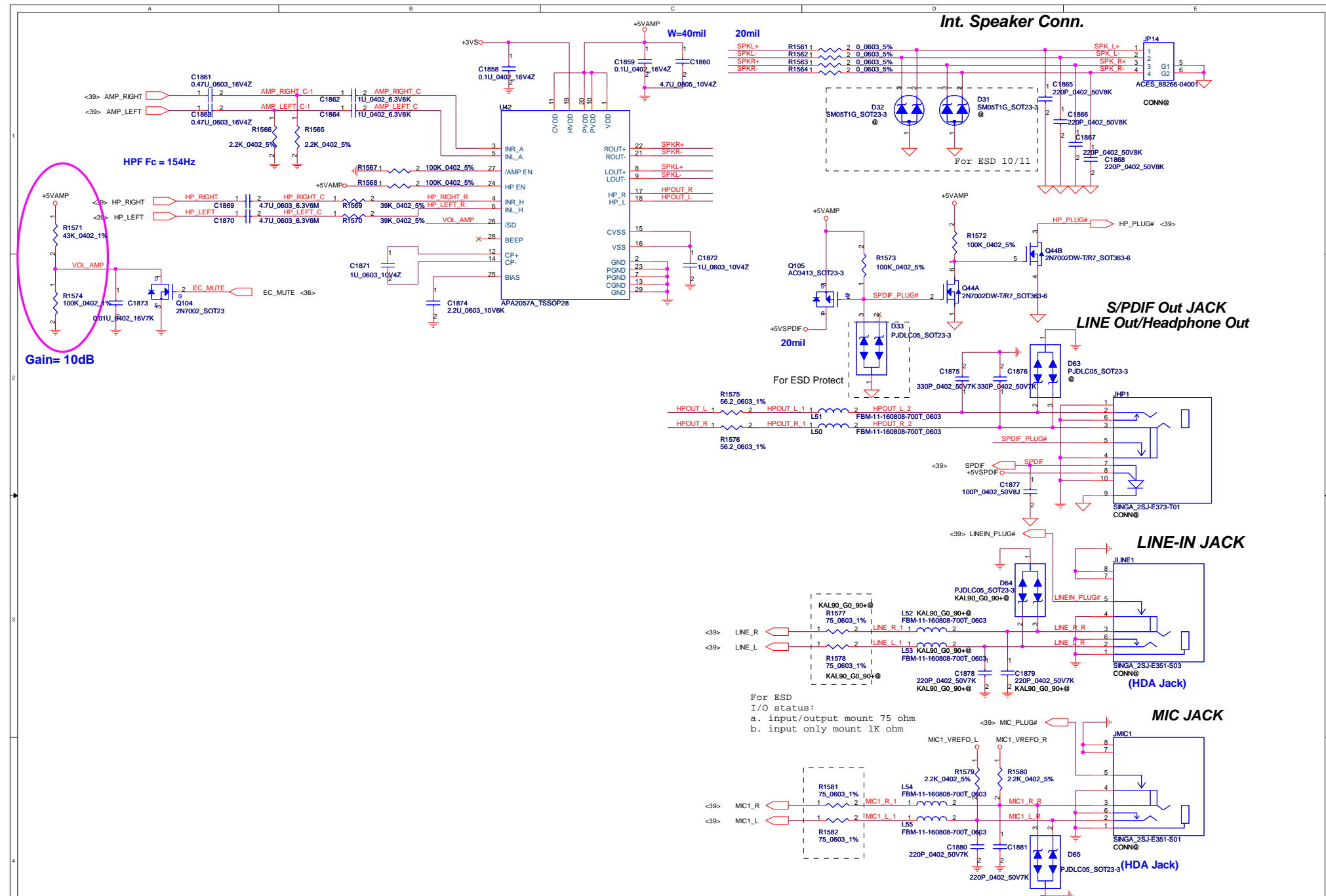


## CIR



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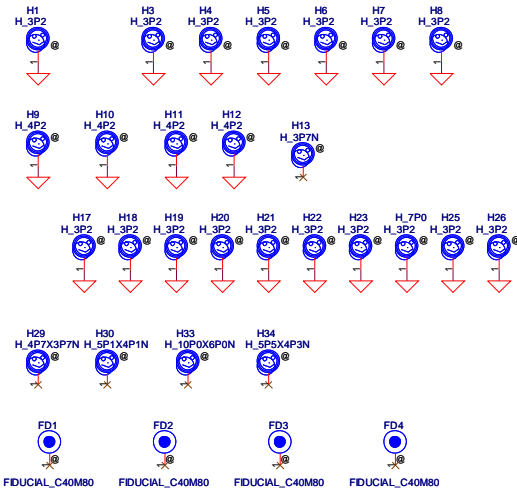
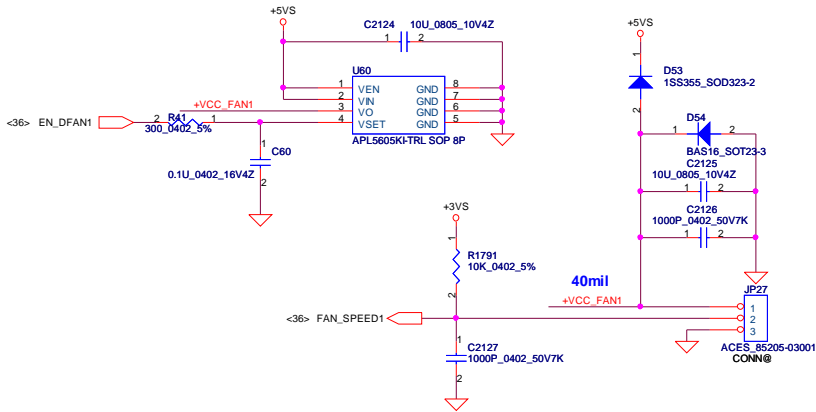




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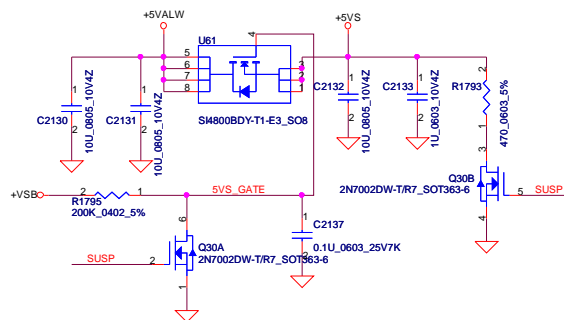


FAN1 Conn

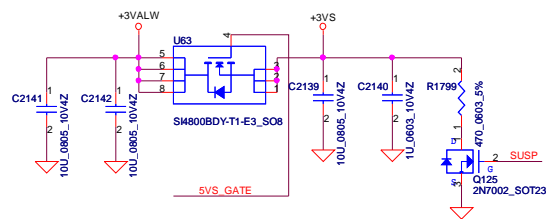


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Size		Document Number			Rev
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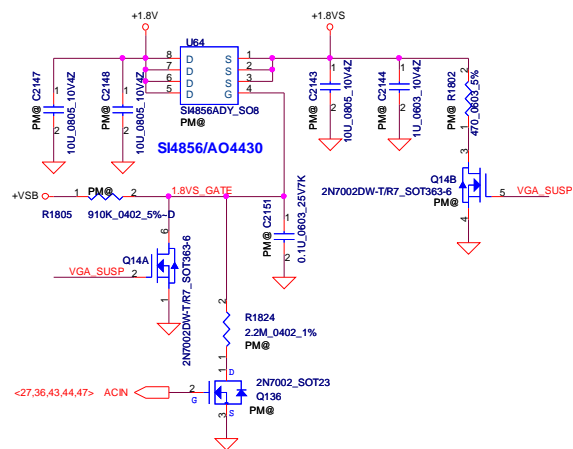
### +5VALW TO +5VS



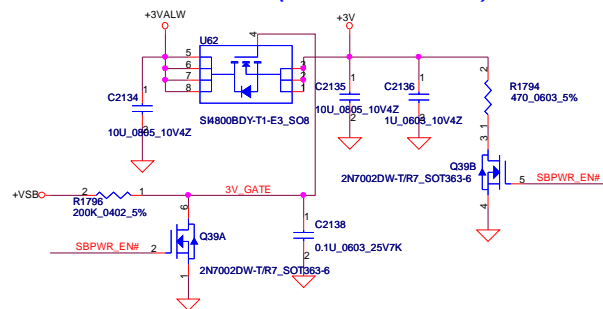
### +3VALW TO +3VS



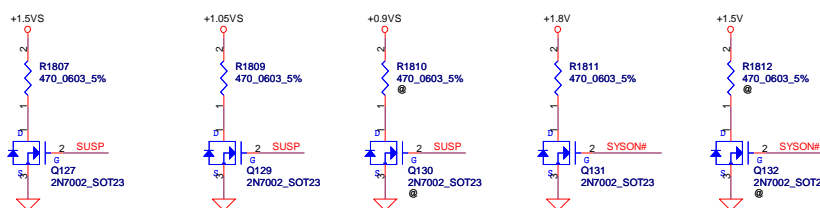
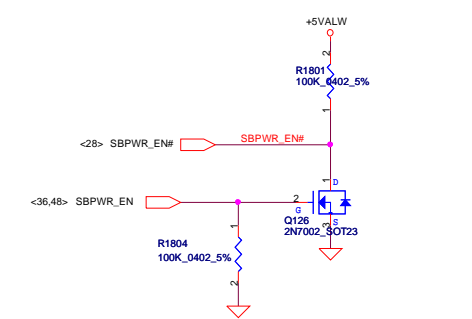
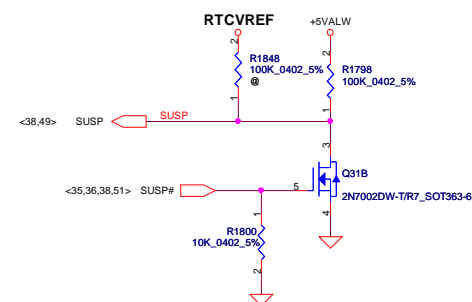
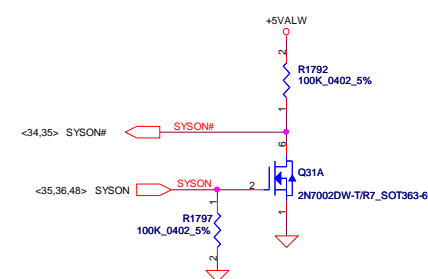
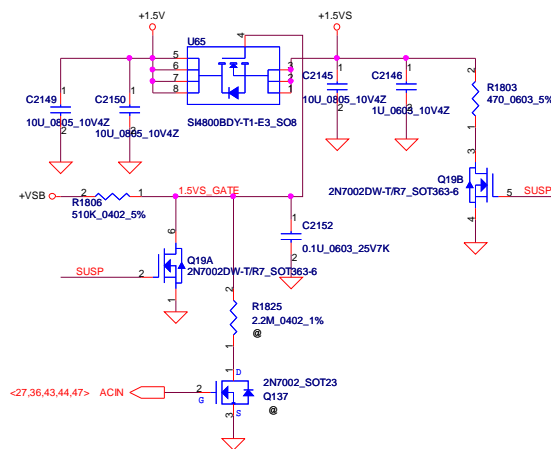
### +1.8V to +1.8VS



### +3VALW TO +3V\_SB(ICH8M AUX Power)

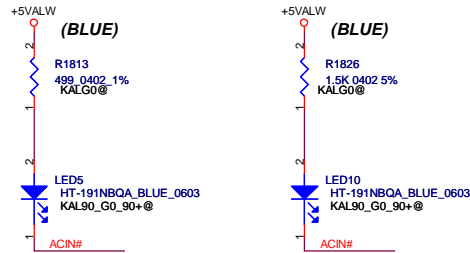


### +1.5V to +1.5VS

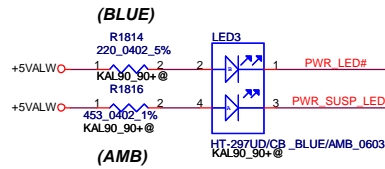


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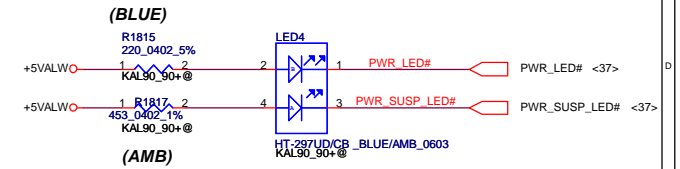
## Enlightener LED



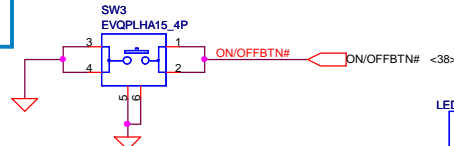
## ON/OFF LED LEFT



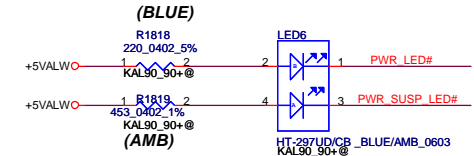
## ON/OFF LED RIGHT



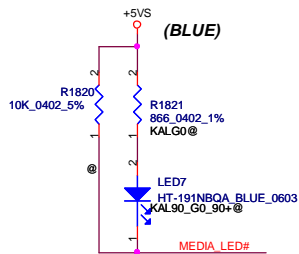
## ON/OFF Button



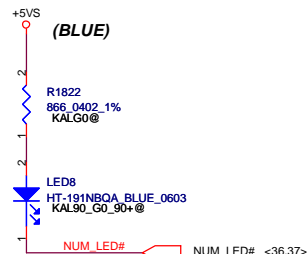
## ON/OFF LED DOWN



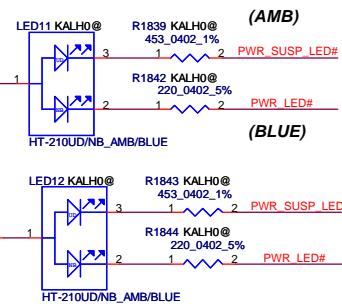
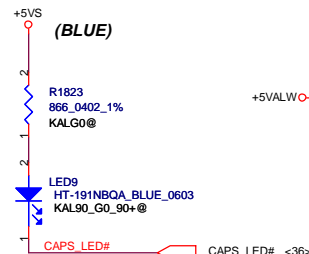
## MEDIA\_LED



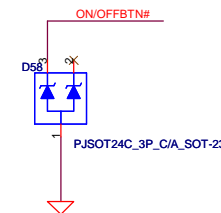
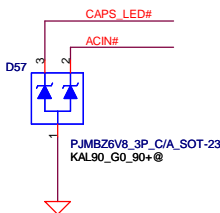
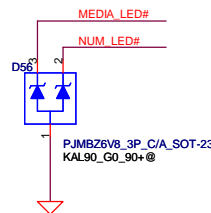
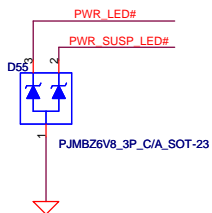
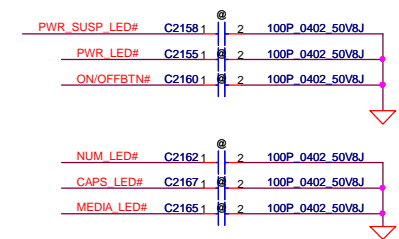
## NUM\_LED



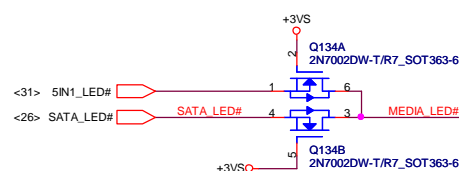
## CAPS\_LED



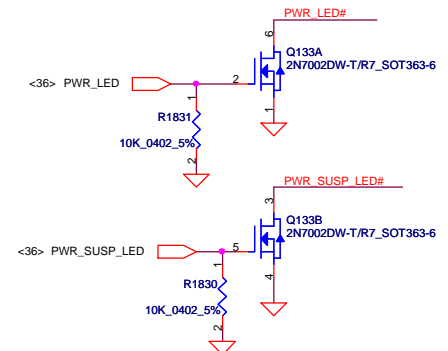
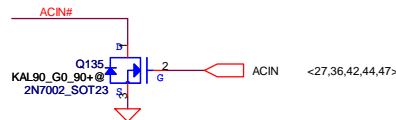
## FOR EMI



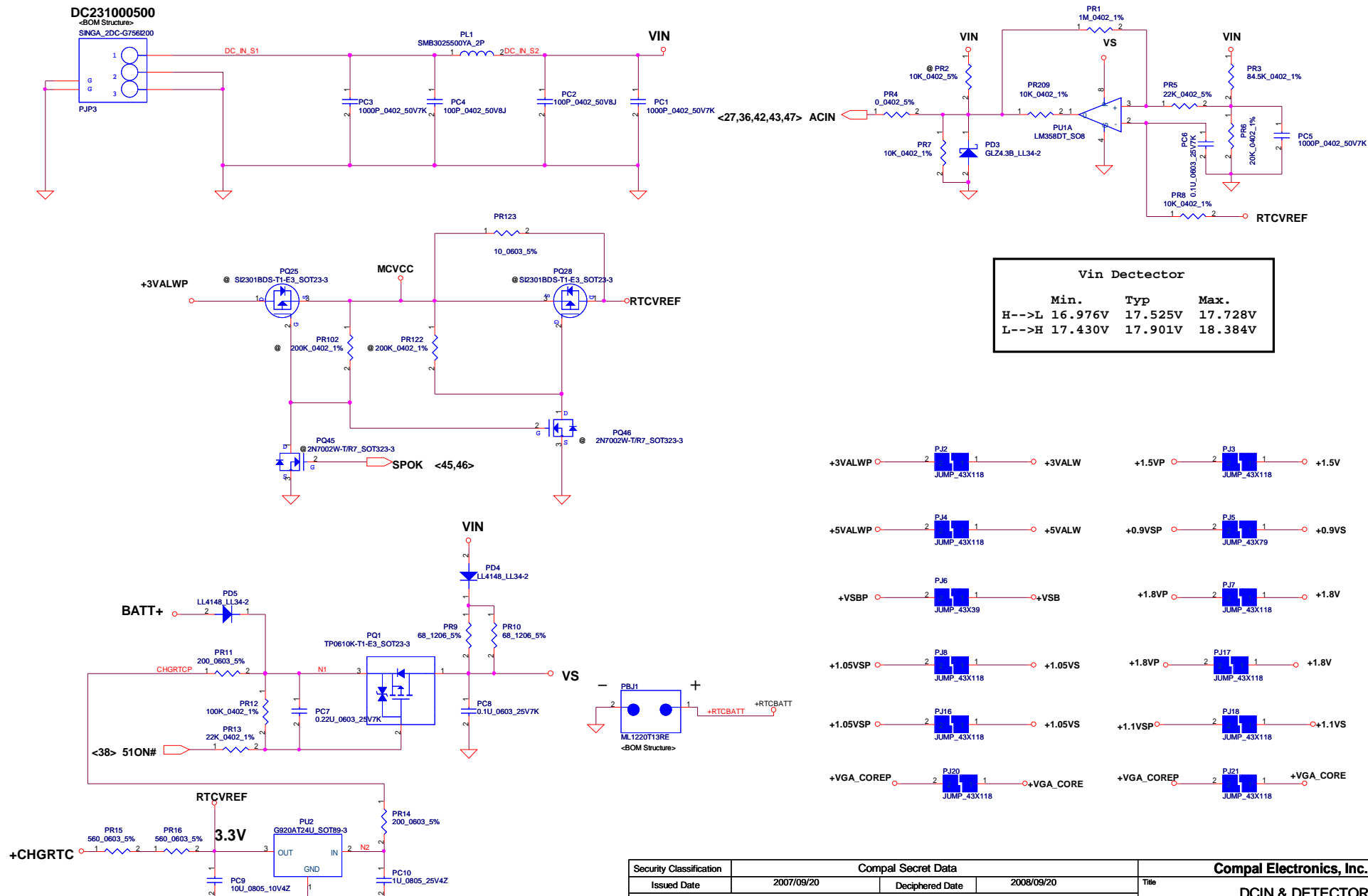
D1 D2 D3 USE PANJIT PJMBZ6V8  
SCA00000100  
6.8V



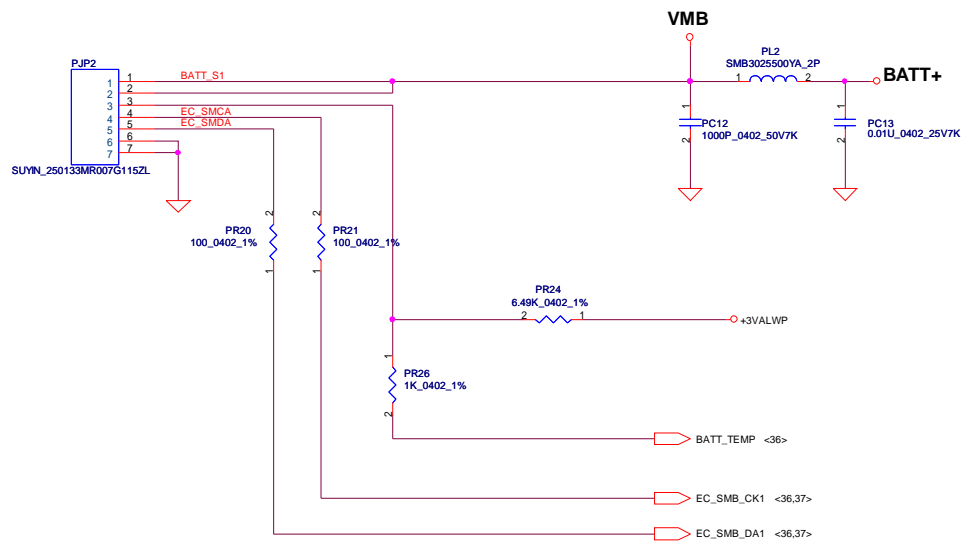
D4 USE  
PJSOT24C 3P C/A SOT-23  
SCA00000E00  
24V



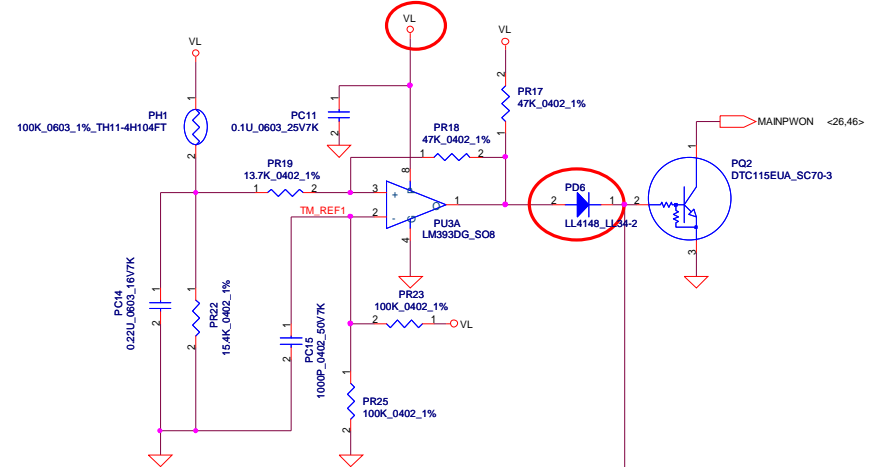
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		Size	Document Number							Rev
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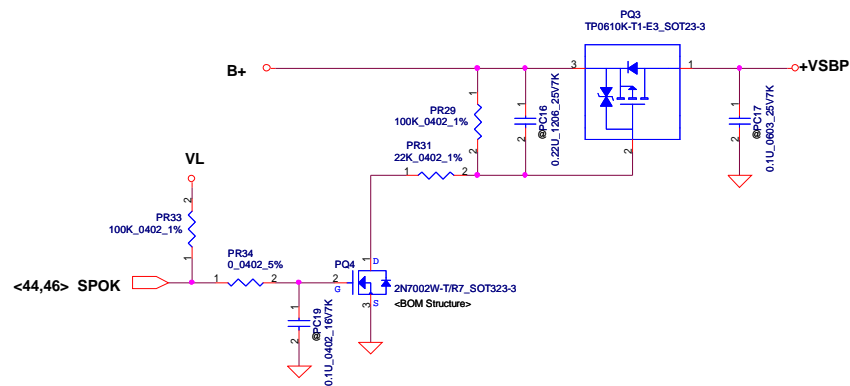
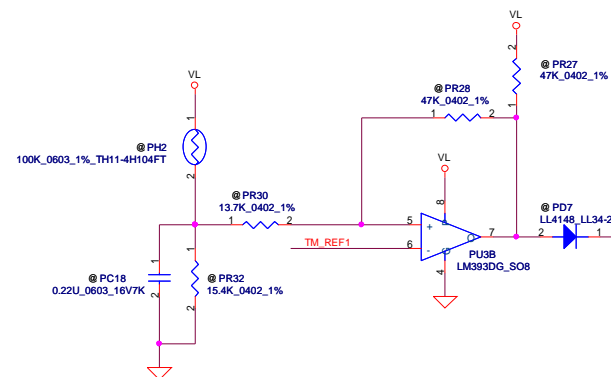
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**PH1 under CPU botten side :**  
 CPU thermal protection at 96 degree C  
 Recovery at 60 degree C

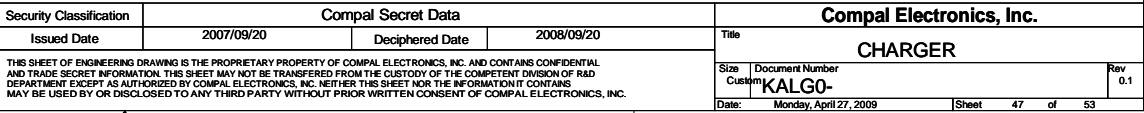


**PH2 near main Battery CONN :**  
 BAT. thermal protection at 79 degree C  
 Recovery at 47 degree C

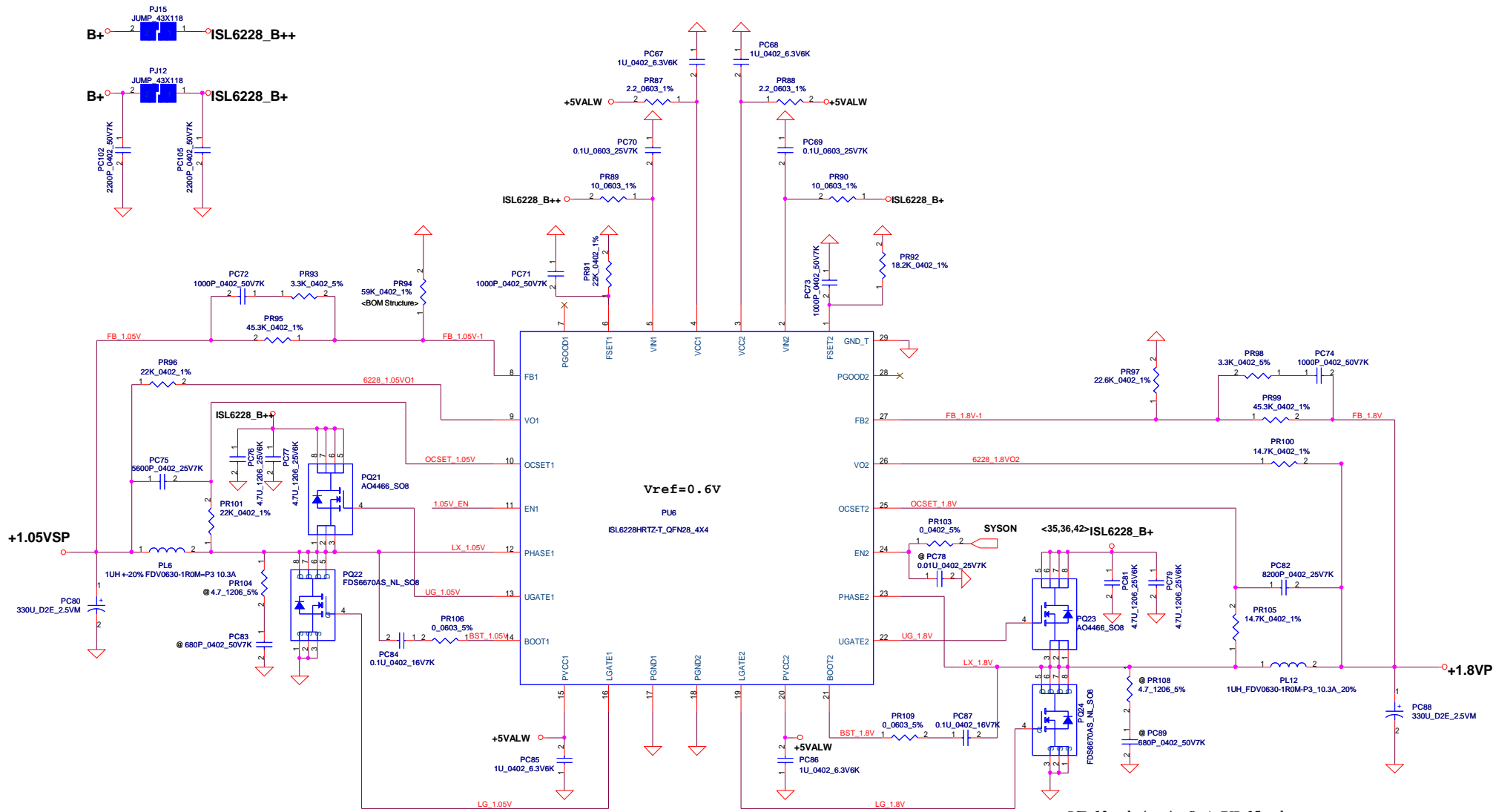


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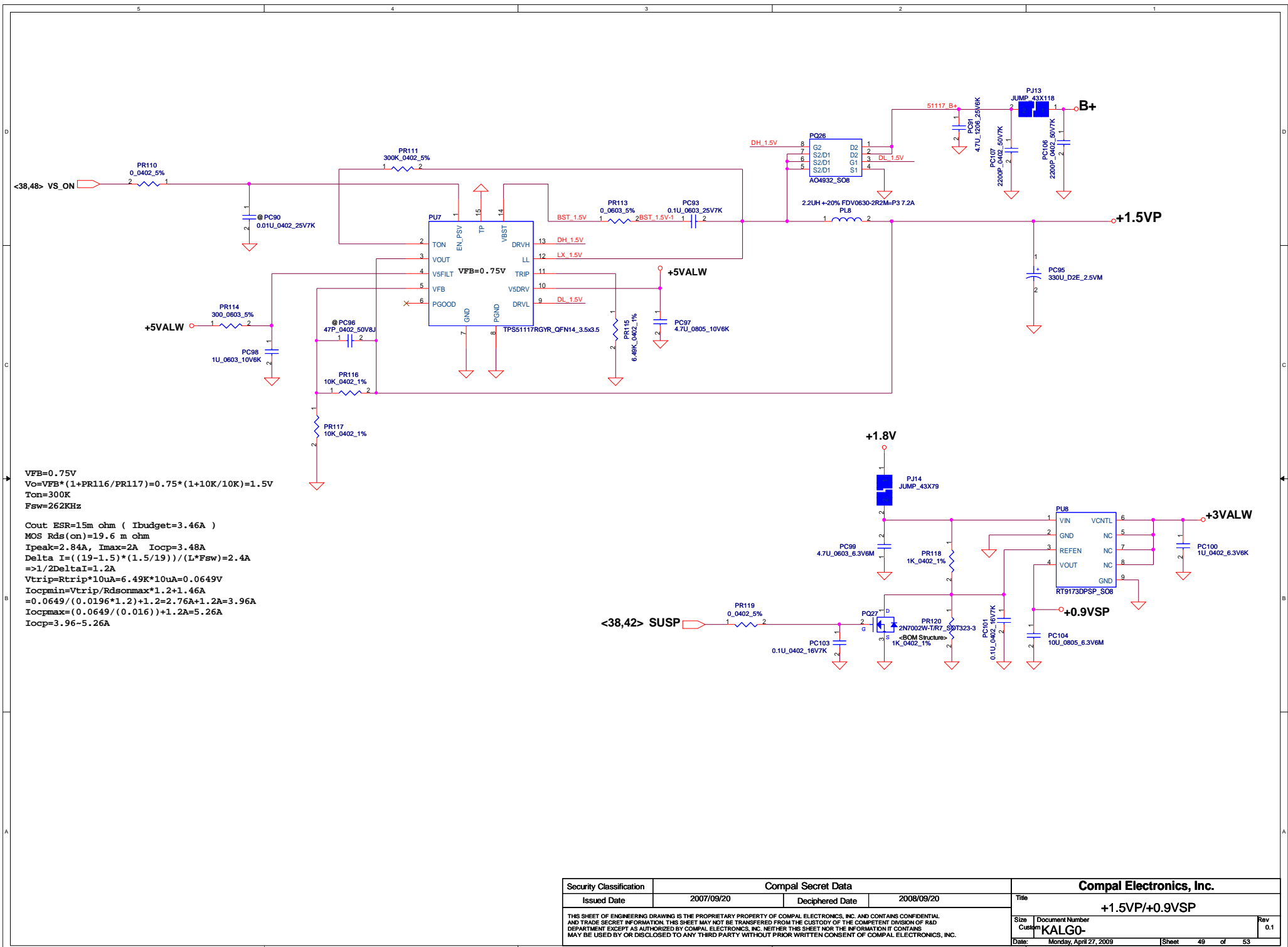
DCR 10m ohm(max) Cout ESR=15m ohm  
 1.05VSP ( Ibudget=17.47A) OCP Setting  
 $F_{sw}=1/1.5E-10*22k=303K$   
 $V_o=V_{ref}*((PR95+PR94)/PR94)$   
 $I_{peak}=13.29A$ ,  $I_{max}=9.31A$   
 $I_{ocp}=13.29*1.2=15.95A$   
 $\Delta I=4.09A$   
 $I_{ocp}*DCR=(Rocset*9.5uA)=(15.95*1.3*10m; Roset=21.8K$   
 now chose Roset=22K  
 $C_{sen}=L/(DCR*Roset)=1uH/(10m*22k); C_{sen}=0.00523uF$   
 now chose  $C_{sen}=5600pF$   
 $I_{ocp\_min}=(22K*9.5uA)/(10m\ ohm*1.3)=16.07A$   
 $I_{ocp\_max}=(22K*10.5uA)/(10m\ ohm)=23.1A$

<36,42> SBPWR\_EN

<38,49> VS\_ON

DCR 10m ohm(max) Cout ESR=15m ohm  
 1.8VSP ( Ibudget=9.91A )  $I_{peak}=9A$ ,  $I_{max}=6.3\ A$   
 $F_{sw}=1/1.5E-10*18.2k=366K$   
 $V_o=V_{ref}*((PR97+PR99)/PR97)$   
 $I_{ocp}=9*1.2=10.8A$   
 $I_{ocp}*DCR=(Rocset*9.5uA)=10.67*1.3*10m; Roset=14.78K$   
 now chose Roset=14.7K  
 $C_{sen}=L/(DCR*Roset)=1uH/(10m*14.7k); C_{sen}=8.16nF$   
 now chose  $C_{sen}=8200pF$   
 $I_{ocp\_min}=(14.7K*9.5uA)/(10m\ ohm*1.3)=10.74A$   
 $I_{ocp\_max}=(14.7*10.5uA)/(10m\ ohm)=15.43A$

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## Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change PR196 value	VGA OCP	0.3	50	change the resistance value of pr196 from 57.6K to 40.2K	2009/02/06	PVT
2	Change PL14 value	prevent OVP occur	0.3	50	change the inductance value of pL14 from 1uH to 0.56 uH	2009/02/06	PVT
3	Change PU4 IC part number	vender suggestion	0.3	45	change part number to SA00002V400	2009/02/06	PVT
4							
5							
6							

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				PIR (PWR)	
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B --> C Change List

0220-----  
Page 6, Change C98 BOM structure to @

0218-----  
Page 20, Add R569 with BOM structure @  
Page 23, R34, R38, R40, R53, R54, R55 change BOM structure to @  
Page 31, Change R215 to 18K  
Update Power Schematics

0213-----  
Page 11, Delete R113  
Add J1 JUMP\_43X79 with BOM structure @  
Page 31, R558, R559 0 ohm with BOM structure @  
R560, R561 4.7K with BOM structure @  
Page 32, R562, R563 0 ohm with BOM Structure @  
R564, R565 0 ohm  
Page 38, Delete C619  
Add R566, R567, R568 0\_0603 with BOM Structure JAL90@

0204-----  
Page 12, Change L31 to MBK1608301YZF\_0603 with BOM structure GM@  
Change R163 to 0\_0805\_5%  
Page 23, Change BOM Structure of U5 to @  
Page 27, Change BOM Structure of R555 and R550 to @  
Page 33, Change R217 to 31.6K\_0402\_1%  
Change C313 to 1U\_0603\_10V6K  
Page 34, Change R503 to FBMA-L10-160808-301LMT\_0603

01/31-----  
Page 23, Delete U10

01/29-----  
Page 23, Change R152 BOM Structure to @

01/24-----  
Page 4, Change U8 to SA00001Z700 (EMC1402)  
Page 33, Change C338 to SE076104K80  
Page 35, Mount C584

01/23-----  
Page 38 Delete F3, R558~560, C609~614

01/22-----  
Page 11, Delete R79  
Change J1 Symbol to JUMP\_43X79  
Page 33, Add R557 10K (Check)  
Change R245 BOM Structure with @  
Page 38, Add C609~614, R558~560 (Check)  
C607,608, 615~619 (Check)

01/17-----  
Page 11, Add R79 0\_0805  
Update Power Schematics

01/16-----  
Page 11, Delete R79 0\_0805  
Add J1 JUMP\_43X79  
Page 16, Change C296, R301 to 27P\_0402  
Page 19, Change L17, L19, L21 BOM structure to GM@  
Page 23, Mount U29, R339  
Add U10 with BOM structure @ (Co-lay with U5)  
Change R340 Bom structure to @  
Change U5 to MX25L4005AMC-12G\_SO8 (SA00002A900)

Page 27, Change U26, C420 BOM structure to @  
Change R550 to 0\_0402  
Add R555 0\_0402  
Page 32, Change R269 to 240\_0402\_5%, R267 to 453\_0402\_1%  
Change R268 pin1 connect to +5VALW  
Page 33, Change R217 to 18K\_0402\_1% with BOM structure PM@  
Page 35, Add R551,R552, R553, R554 75\_0603\_1% with BOM structure JAL90@  
Add D32 PJDLC05\_SOT23-3  
Page 38, Add F3 3A\_15VDC\_SMD2920P300TF/15  
Page 49, Add R551,R552, R553, R554 1K\_0603\_1% with BOM structure 268@  
Add L17, L19, L21 0\_0805 with BOM structure PM@  
Update U38 (ALC268-VB1-GR ) PN: SA00001GD10 for JAW50

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